Bridging Hardware and Software Analysis with Btor2C: A Word-Level-Circuit-to-C Translator

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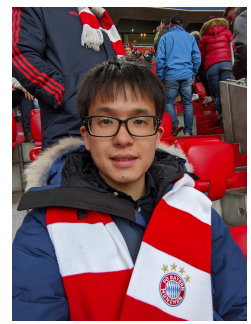

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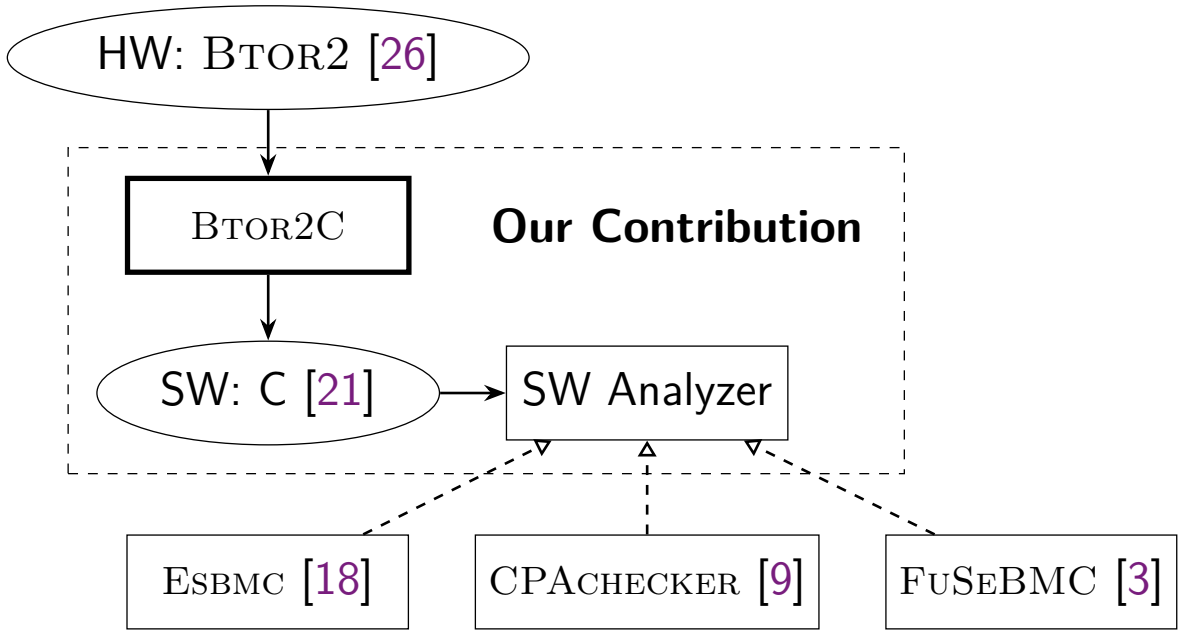
SoSy-Lab Software Systems

About this talk



- **43** HW-verification tasks uniquely solved by SW analyzers in our evaluation

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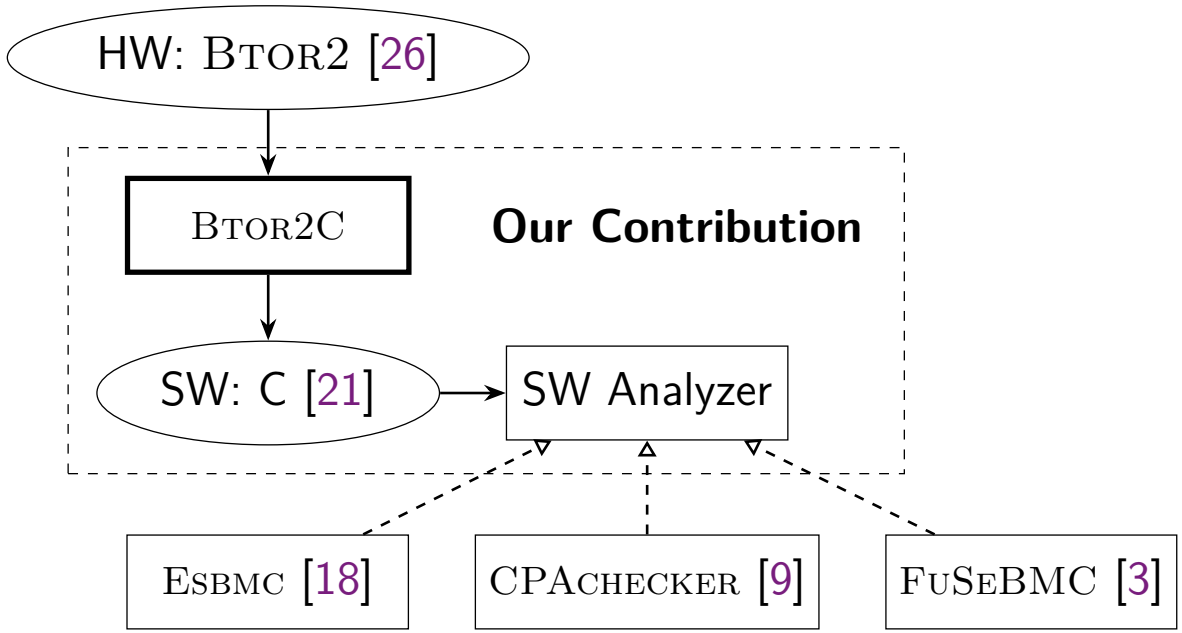
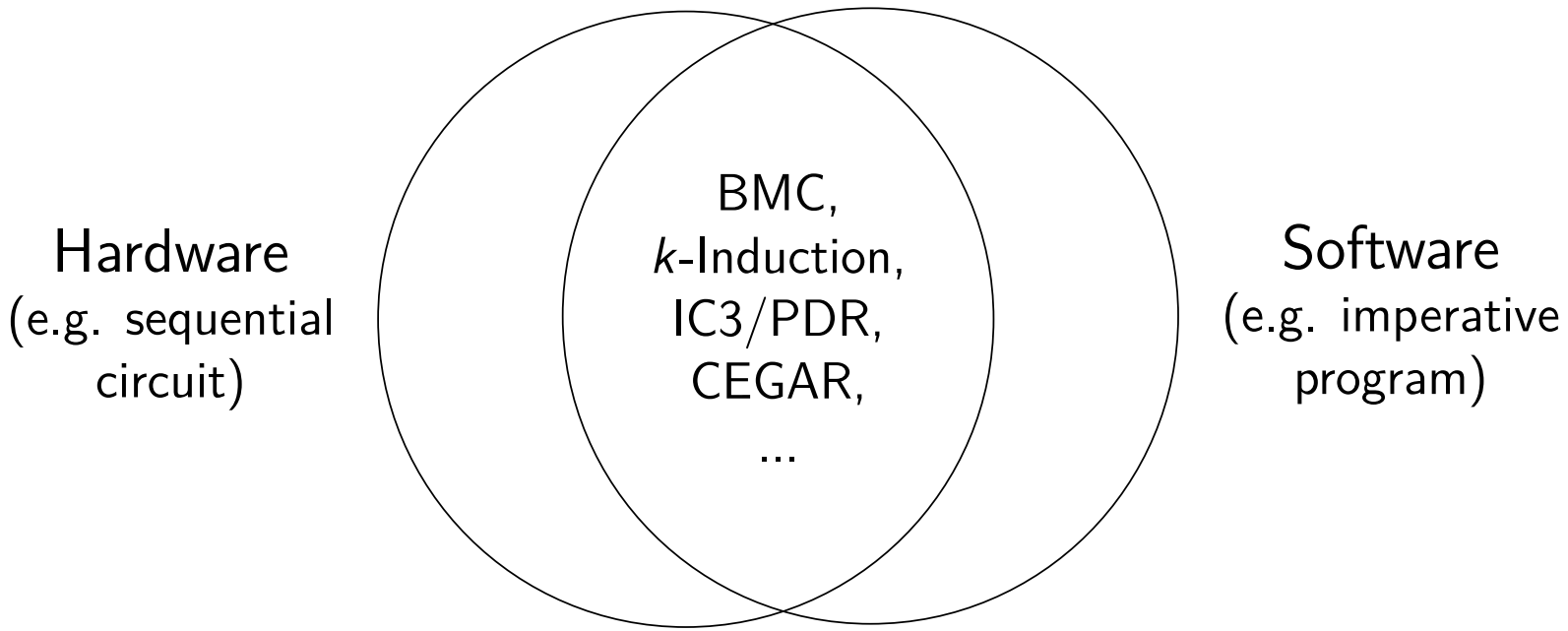


- **43** HW-verification tasks uniquely solved by SW analyzers in our evaluation → enhance HW quality assurance

Outline

Analysis of Computational Systems

- Quality assurance is important for computational systems
- Analysis methods are usually developed for a specific model
- Theoretical foundations and technologies are shared



Analysis Algorithms for HW and SW

- HW-verification algorithms adopted for SW
  - BMC [12]
  - *k*-Induction [27]
  - IC3/PDR [13, 8]
- SW-testing algorithms adopted for HW
  - Fuzzing [23]
  - Symbolic execution [22]

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- SW-testing algorithms adopted for HW
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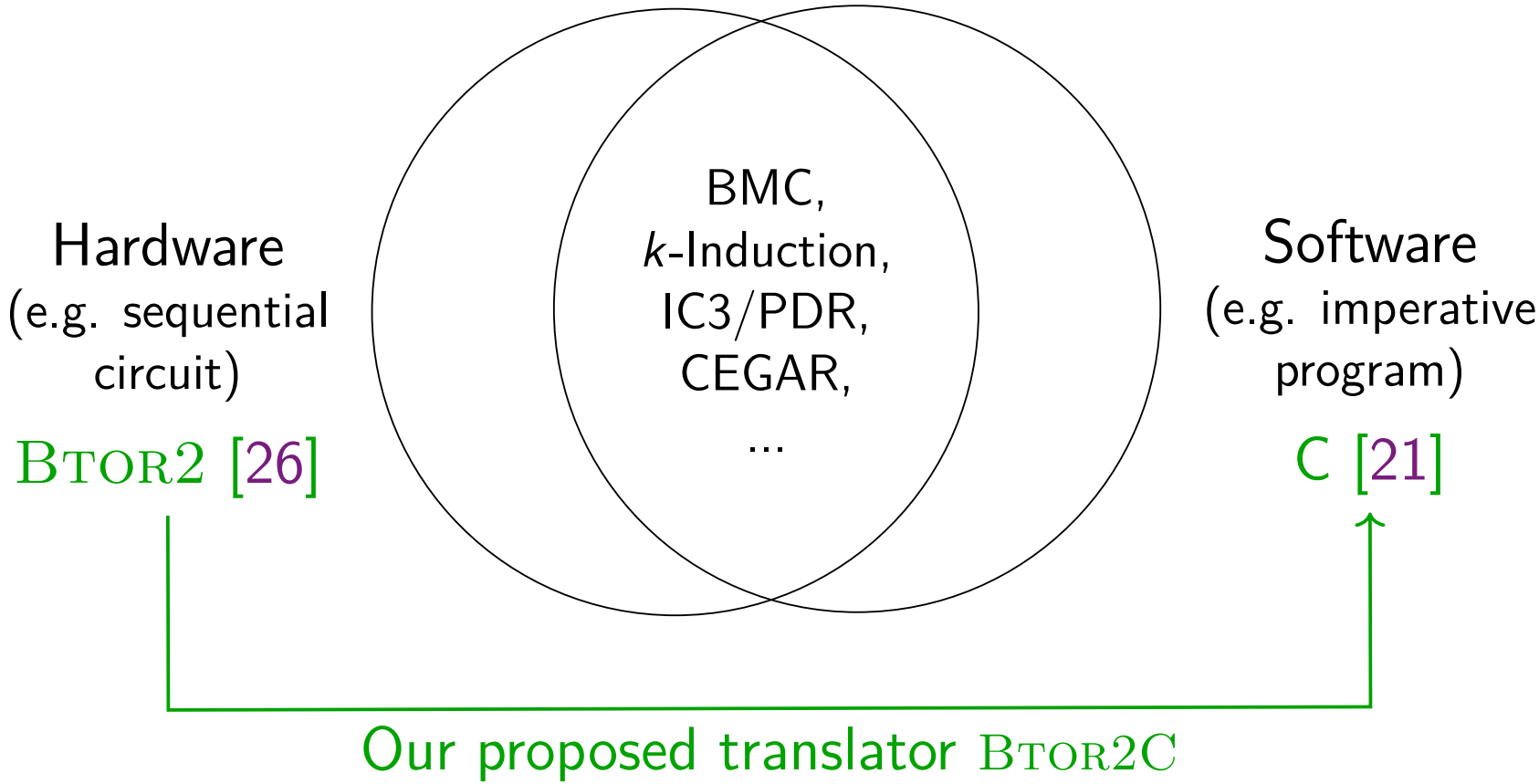
  - Symbolic execution [22]
- Leveraging knowledge from one field to another is **difficult**

Bridging the Gap between HW and SW Analysis



Design Decisions

- Why BTOR2 as frontend?
- Why C as target?
- Why a standalone translator?

Why BTOR2 as Frontend?

- Simple yet expressive
  - A word-level extension to the bit-level format AIGER [10]
  - Bit-precise language for hardware-verification problems
  - Much simpler than Verilog [1]

Why BTOR2 as Frontend?

- Simple yet expressive
  - A word-level extension to the bit-level format AIGER [10]
  - Bit-precise language for hardware-verification problems
  - Much simpler than Verilog [1]
- Extensive tool support
  - Utility tool suite BTOR2TOOLS [25] available
  - YOSYS [28] supports translation from Verilog to BTOR2
  - Used in HWMCC [11] $\Rightarrow$ Supported by many hardware model checkers (and many benchmark tasks available)

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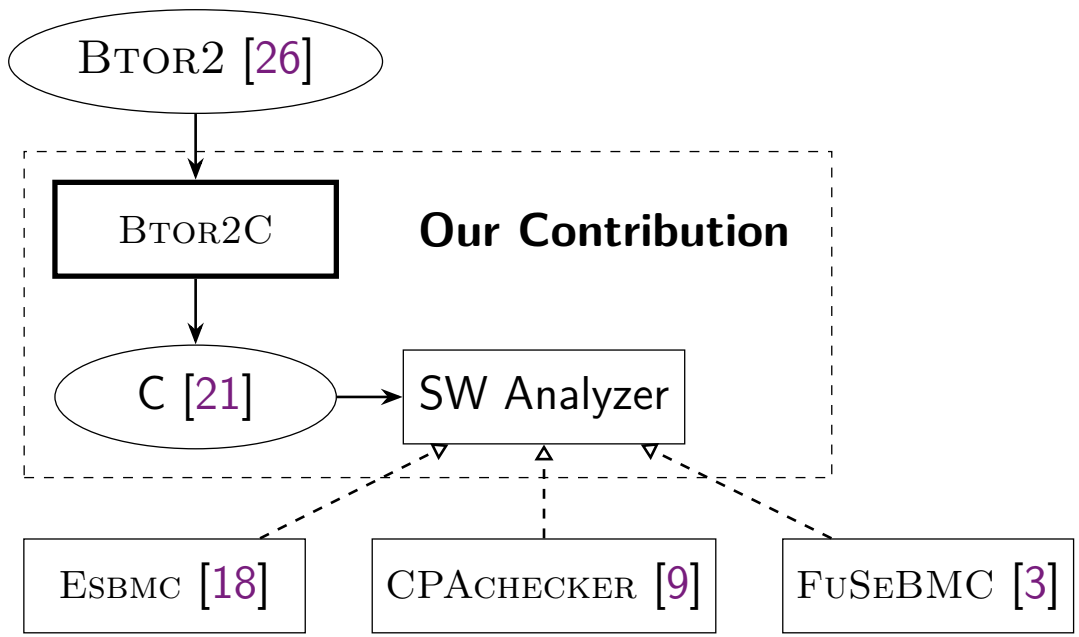
Why C as target?

Analysis Tool Chain



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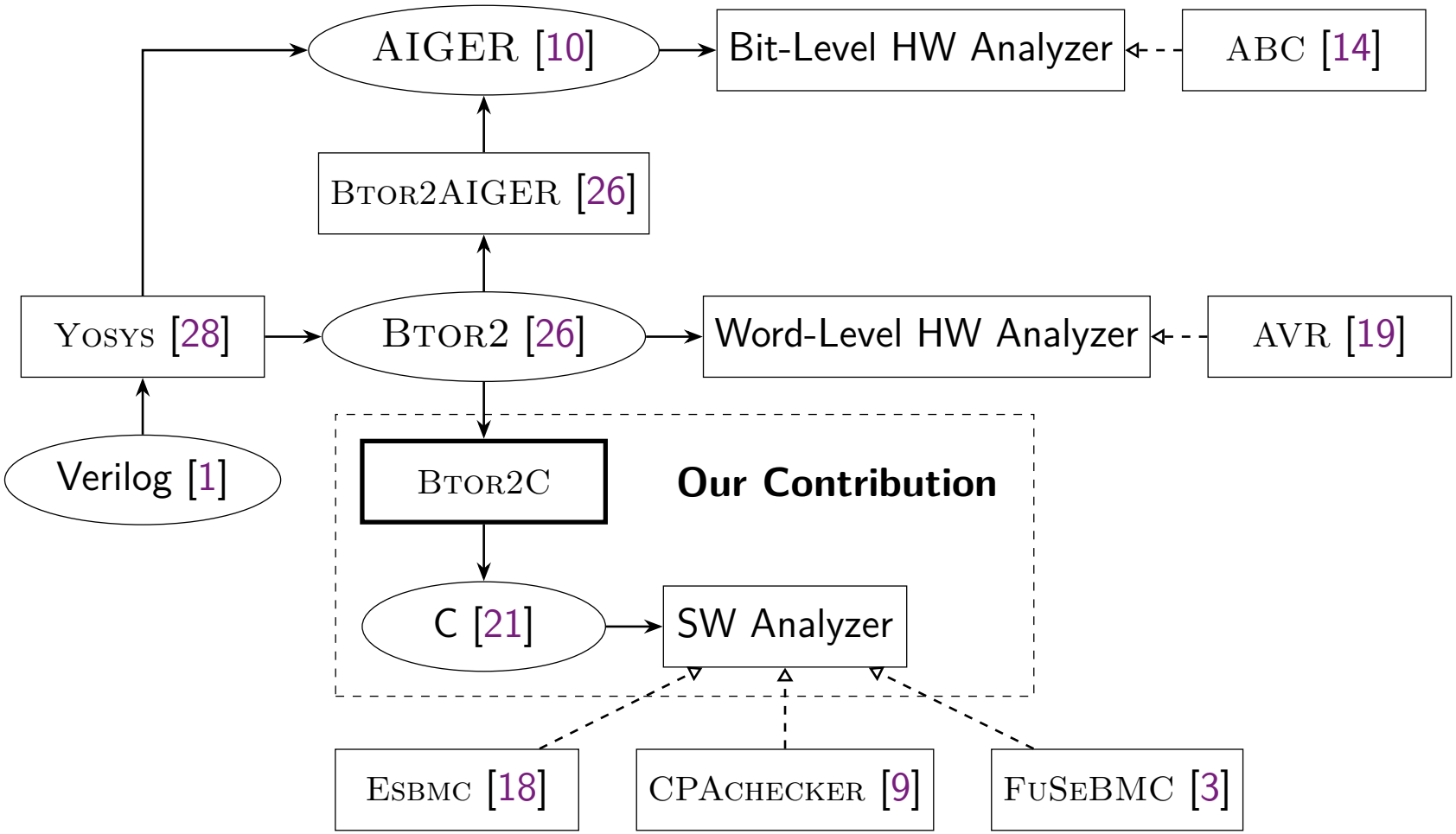

What can Btor2C do for you?

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What can Btor2C do for you?

- For HW designers
  - Enhance quality assurance by utilizing SW analyzers
- For developers of SW analyzers
  - Evaluate their algorithms and implementations on HW-verification problems
  - 1224 translated tasks have been contributed to SV-COMP '23 benchmark set

Model-Checking Problem of Reachability Safety

Problem formulation

- For hardware:
  decide whether the safety property holds on all executions of the sequential circuit
- For software:
  decide whether there is an executable program path that reaches the *error* location

The BTOR2 Language

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12 eq 11 3 10
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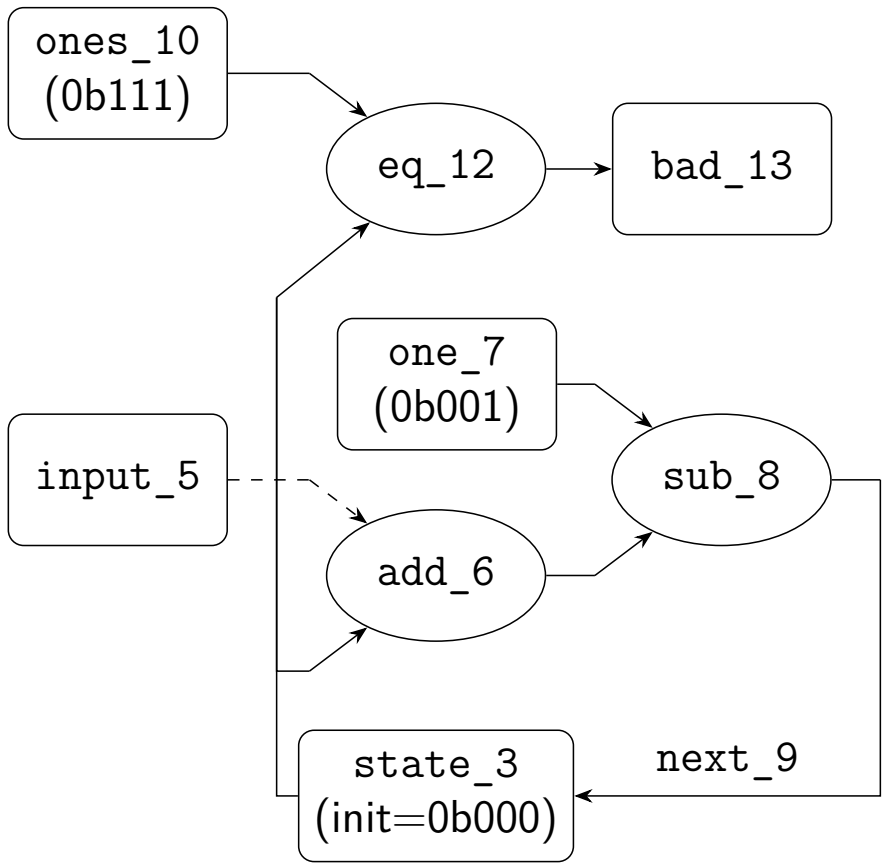

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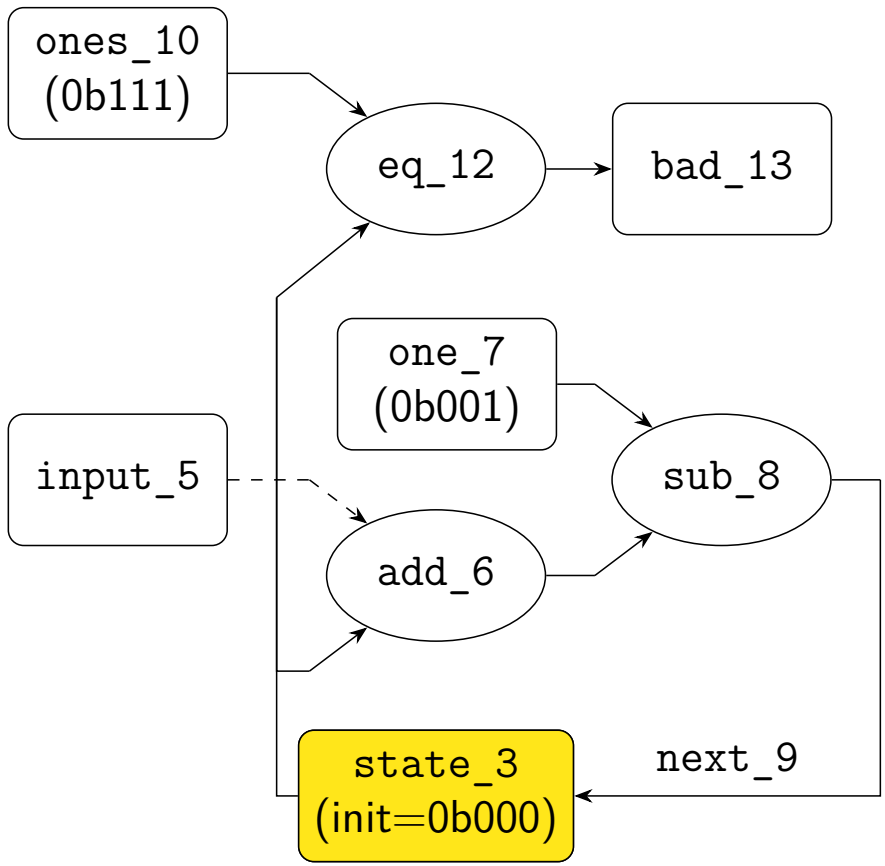

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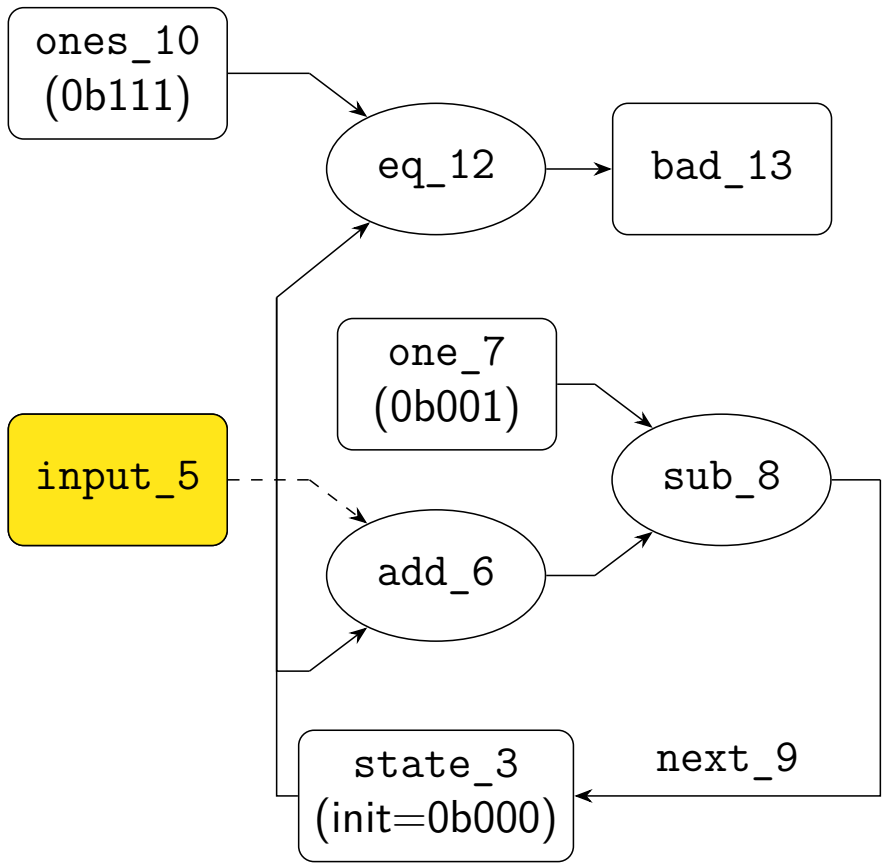

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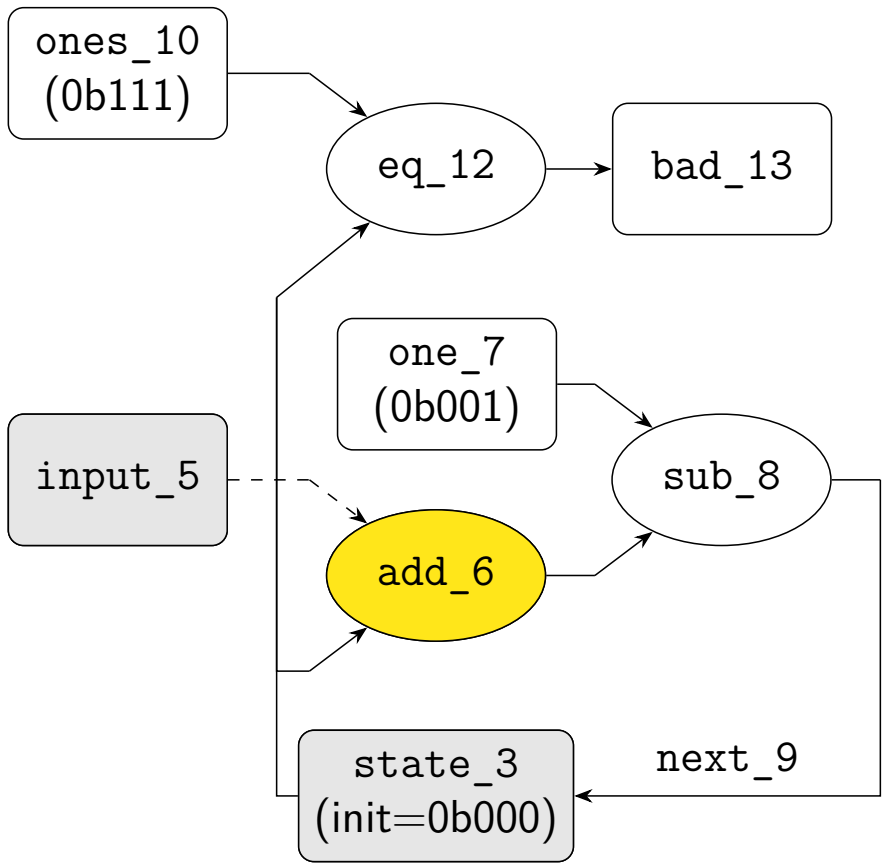

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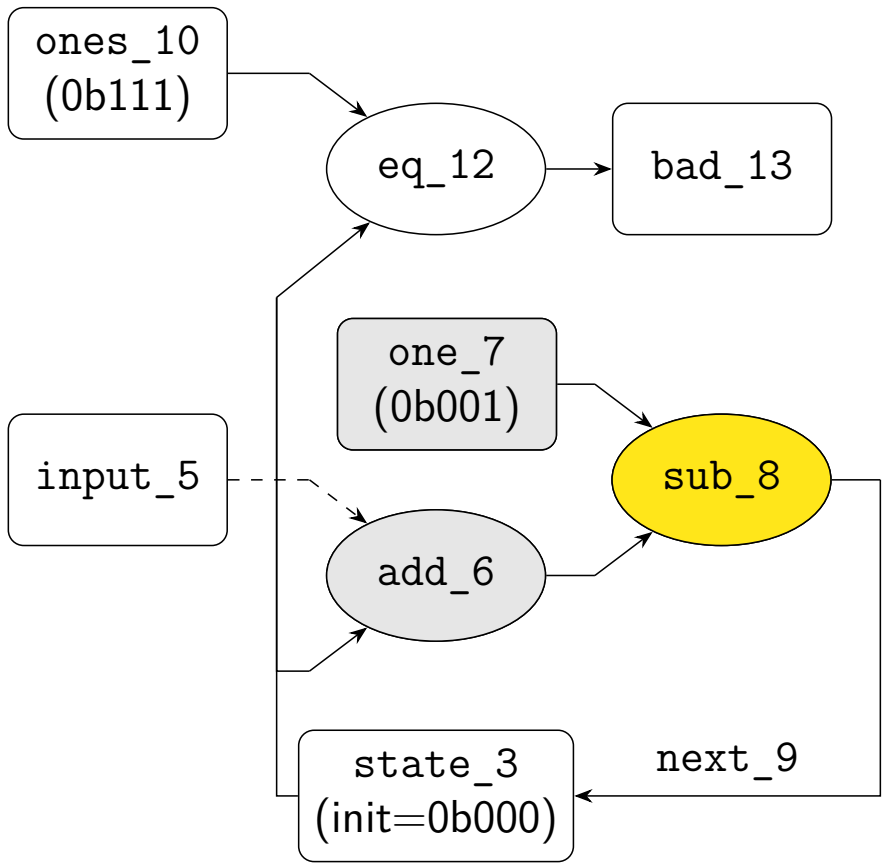

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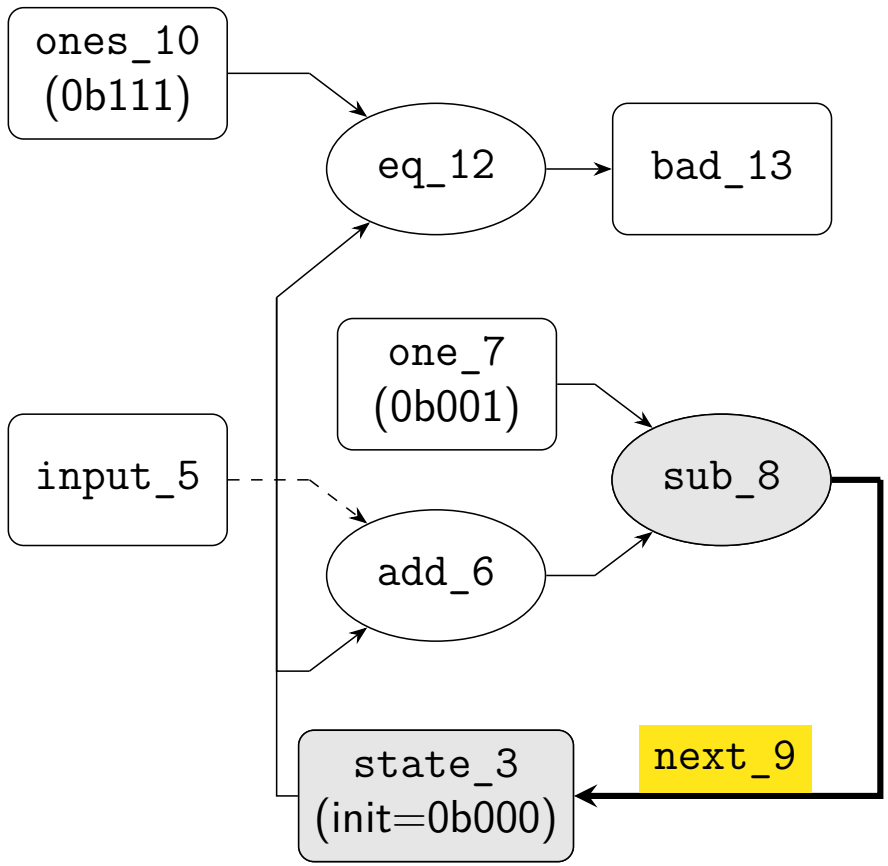

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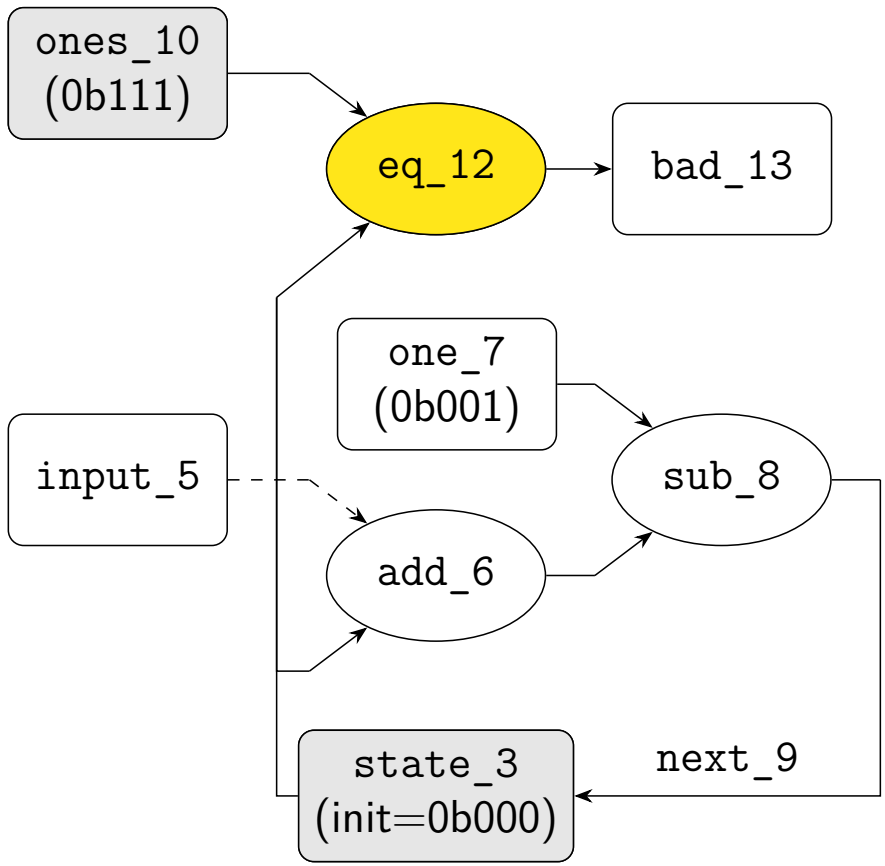

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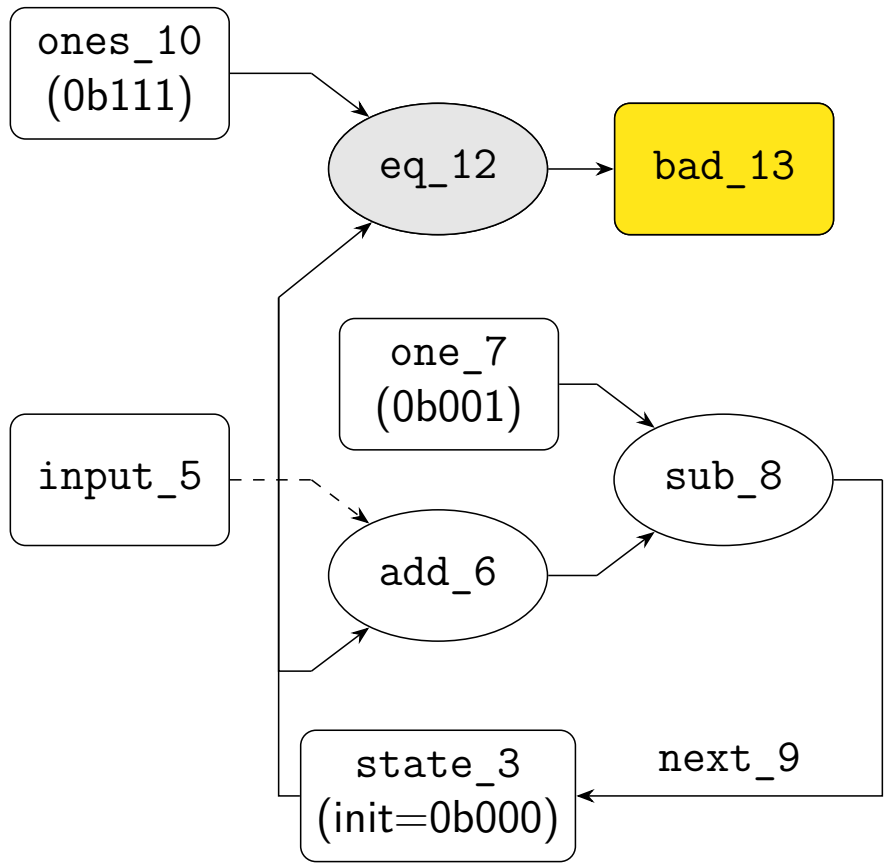

Simulating Sequential Circuits with C Programs

A generic program template:

```
1  void main() {
2    // Define sorts and constants
3    // Initialize states
4    for (;;) {
5      // Get external inputs
6      // Evaluate safety property
7      if (bad) {
8        ERROR: abort();
9      }
10     // Compute and assign next states
11   }
12 }
```

Translating BTOR2 to C

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4    const SORT_1 var_2 = 0b000;
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Encoding BTOR2 Sorts with C

BTOR2 sorts	C types
`bitvec`	`unsigned {char,short,int,long}` e.g. `sort bitvec 3` → `unsigned char` mask spare bits: `c_var & 0b111`
`array`	static array, e.g. `unsigned int [][]`

Modeling BTOR2 Constructs with C

BTOR2	C
`input`	non-deterministic function
`bad`	`if` guard with an `ERROR` label
`state`	C var in scope `main`
`init`	initialize state var before entering `for`
`next`	update state var at the end of `for`

Implementing BTOR2 Operators in C

A typical line in BTOR2:

```
<nid0> <op> <sid> <nid1> [<nid2 [nid3]>]
```

BTOR2	C
`a add x b c`	`SORT_x var_a = var_b + var_c;`
`a and x b c`	`SORT_x var_a = var_b & var_c;`
`a ite x b c d`	`SORT_x var_a = var_b ? var_c : var_d;`
`a concat x b c`	`SORT_x var_a = var_b << N | var_c;` (`N` is the bit-width of `var_c`)
`a udiv x b c`	`SORT_x var_a = (var_c == 0) ? MAX_VAL : (var_b / var_c);` (`MAX_VAL` is the max value of `SORT_x`)

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  - **lazily**: only when precise values are needed
- The latter yields better performance in our experiments

Revisit: Translating BTOR2 to C

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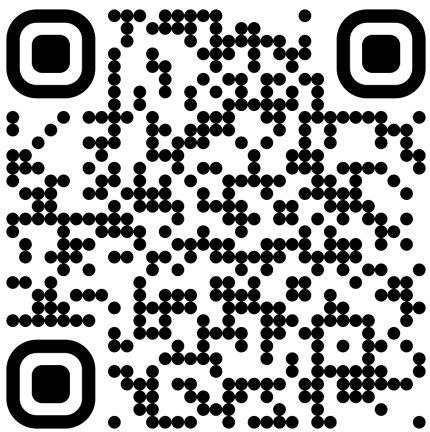
Implementation

- A lightweight translator Btor2C
  - Written in C with ∼1600 LOC
  - Use the frontend parser provided by Btor2Tools [25]
  - Compiled binary < 0.25 MB
- Open-source under Apache License 2.0

https://gitlab.com/sosy-lab/software/btor2c



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- **RQ2**: How do SW analyzers perform on HWMCC tasks?
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- **RQ3**: Can SW analyzers complement HW model checkers?
  *Yes, **43** tasks were uniquely solved by SW verifiers*

State-of-the-art Analyzers

The following tools/algorithms were evaluated

- Winners of HWMCC '20
  - ABC [14] (bit-level): PDR
  - AVR [19] (word-level): PDR
- Top winners of *ReachSafety* category in SV-COMP '22
  - CPAchecker [9]: Predicate Abstraction
  - Esbmc [18]: *k*-Induction
  - VeriAbs [2]: Loop Abstraction + BMC
- Overall winner of Test-Comp '22
  - FuSeBMC [3]: Fuzzing + BMC

Benchmark Set

- Collected from HWMCC '19 and '20
- Total 1498 BTOR2 tasks

	Safe	Unsafe	Total
Bit-vector	868	473	1341
(BV+) Array	140	17	157

- Translation to other formats
  - → AIGER by BTOR2AIGER (array not supported)
  - → C by BTOR2C

Experimental Setup

- OS: Ubuntu 22.04 (64 bit)
- Machine: 3.4 GHz CPU (8 cores) and 33 GB of RAM
- Each task is limited to
  - 2 CPU cores
  - 15 min of CPU time
  - 15 GB of RAM

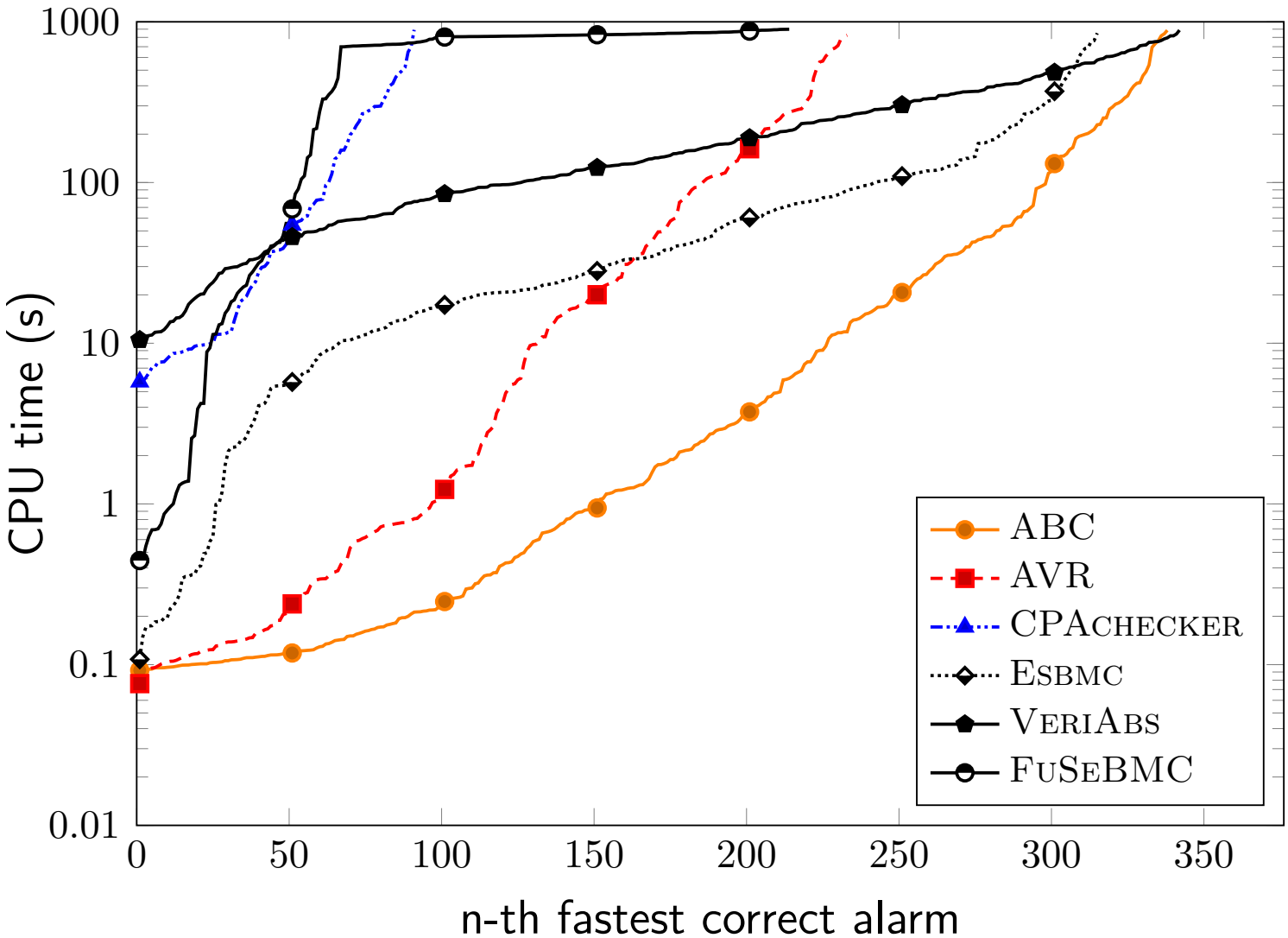
  (reliable resource management by BenchExec[1])

[1] https://github.com/sosy-lab/benchexec

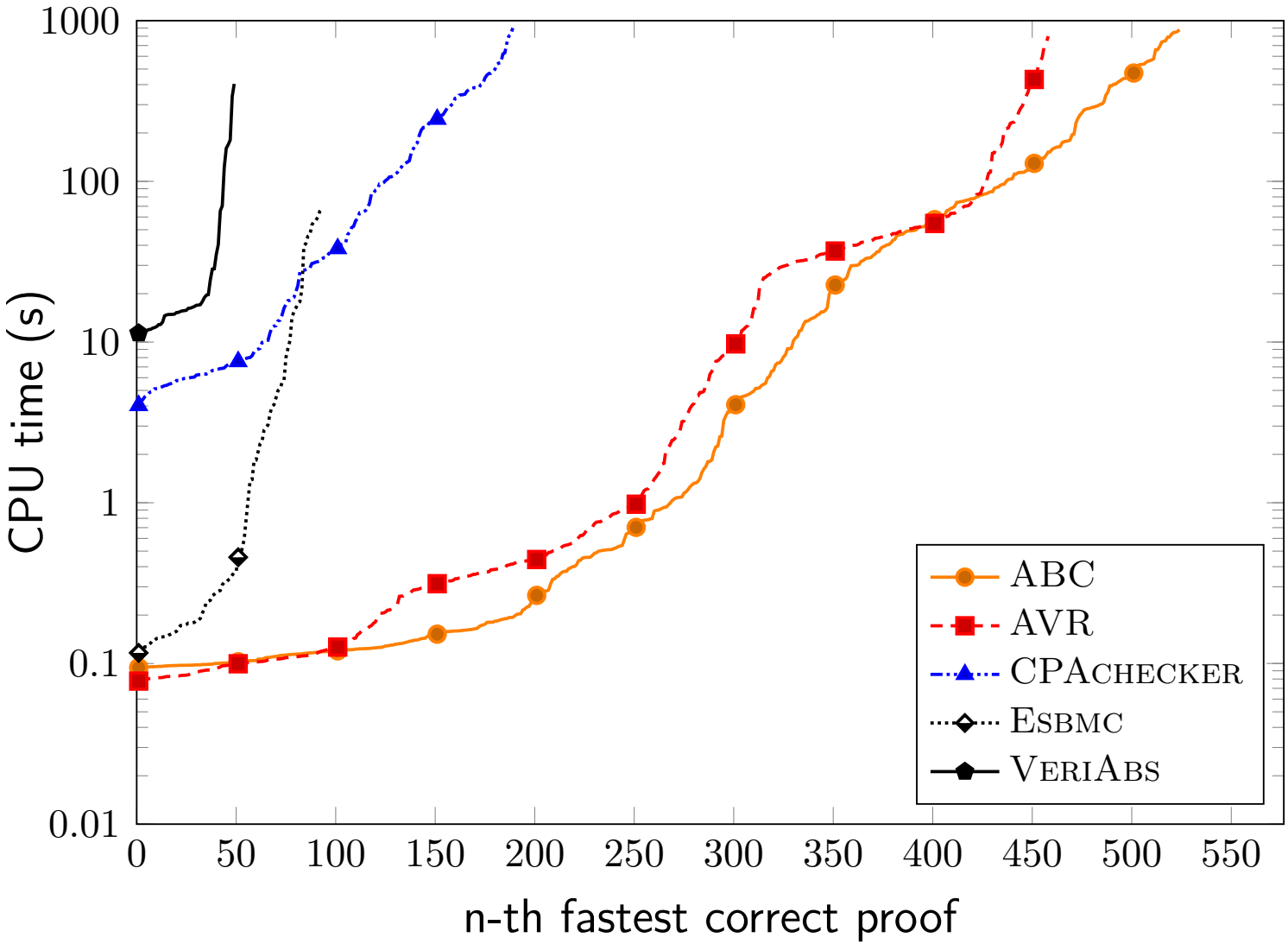
Overall Results

Tool	ABC	AVR	CPAchecker	ESBMC	VeriAbs
Algorithm	PDR	PDR	PA	KI	LA
Input	AIGER	Btor2	C (bit-masking applied lazily)		
Correct results	**862**	736	280	**410**	393
BV proofs	**524**	458	**189**	93	49
BV alarms	**338**	233	91	315	**342**
Array proofs	–	**45**	0	0	0
Array alarms	–	0	0	**2**	**2**
Wrong proofs	0	0	0	0	2
Wrong alarms	0	0	0	0	1
Timeouts	479	559	922	551	1 042
Out of memory	0	3	7	537	4
Other inconclusive	0	200	289	0	56

Quantile Plot: Unsafe Bit-vector Tasks



Quantile Plot: Safe Bit-vector Tasks



Reasons for Performace Difference

- Input: AIGER vs. Btor2 vs. C (with spare bits)
- Representation: transition system vs. control-flow graph
- Backend logical solver
  - ABC: SAT solver
  - Others: SMT solver

Analyzer	Solver
AVR	Yices2 [17]
CPAchecker	MathSAT5 [16]
Esbmc	Boolector3 [26]

Conclusion

- BTOR2C translates BTOR2 circuits to C programs
- With BTOR2C, we can
  - Utilize off-the-shelf software analyzers to check the correctness of hardware designs
  - Improve quality assurance for hardware systems
- In our evaluation, software verifiers were able to solve **43** tasks that hardware verifiers cannot
- The reproduction artifact [6, 7] is available via Zenodo

Future Work

- Improve Btor2C
  - Avoid redundant array copies during `write`
  - Support witness format conversion

Future Work

- Improve Btor2C
  - Avoid redundant array copies during `write`
  - Support witness format conversion
- Bridge the gap from the other direction
  - Translate SW to HW

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Related Work

- Translating hardware to software
  - V2C [24] translates Verilog to C
  - BTOR2LLVM[1] and BTOR2CHC[2] translate BTOR2 to LLVM-IR and Constrained Horn Clauses, respectively
- Compiling hardware to intermediate representation
  - YOSYS [28] translates Verilog to AIGER and BTOR2
  - QUTERTL [29] translates Verilog/VHDL to BTOR
  - VERILOG2SMV [20] compiles Verilog into SMV [15]

[1] https://github.com/stepwise-alan/btor2llvm
[2] https://github.com/stepwise-alan/btor2chc

The BTOR2 Language

```
1 sort bitvec 3
2 zero 1
3 state 1
4 init 1 3 2
5 input 1
6 add 1 3 5
7 one 1
8 sub 1 6 7
9 next 1 3 8
10 ones 1
11 sort bitvec 1
12 eq 11 3 10
13 bad 12
```

- Each line starts with a unique index (variable id)
- `sort`: `bitvec` or `array`
- `input`: external input to the circuit
- Registers and memories:
  - `state`: declare a state variable
  - `init`/`next`: initialize/update
- `bad`: bad state property
- Constants: `zero`, `one(s)`, `const`
- Operators: `add`, `sub`, `eq`, ...

Limitations

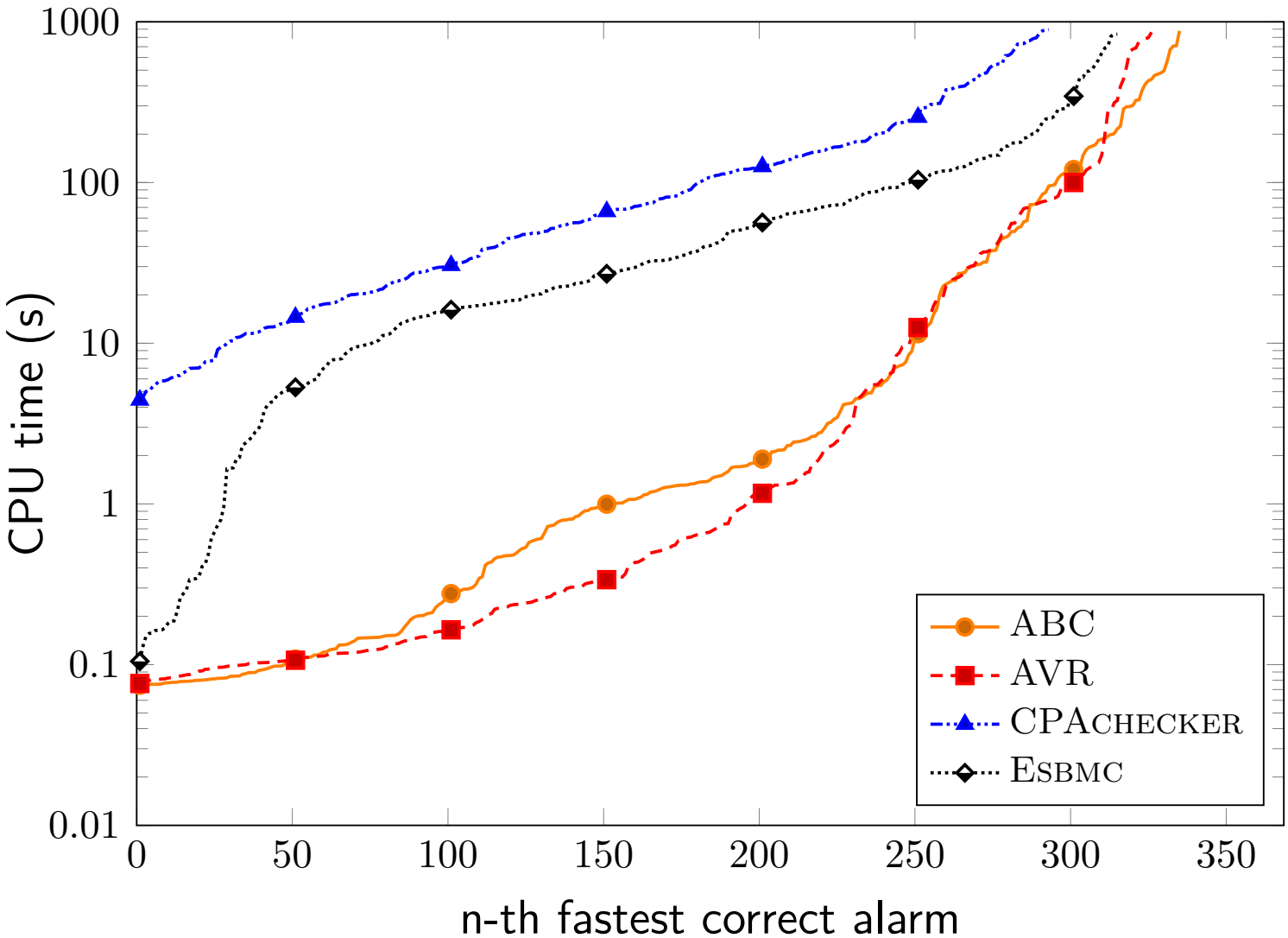
Unsupported BTOR2 features

- Bit-vector sort of size larger than 64 bits
- Fairness constrains: `fair`
- Liveness properties: `justice`
- Overflow detection: `{add,div,mul,sub}o`

Benchmark Sources

- Microprocessor
  - picoJava
  - RIDECORE (RISC-V)
- Application
  - Cyclic redundancy check
  - Huffman coding
  - mutual exclusion
- Industry

Quantile Plot: Comparing BMC Implementations



ESBMC-KI vs. AVR-KI