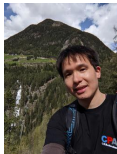


Bridging Hardware and Software Formal Verification for Reliable Computing Systems

Nian-Ze Lee

LMU Munich, Germany

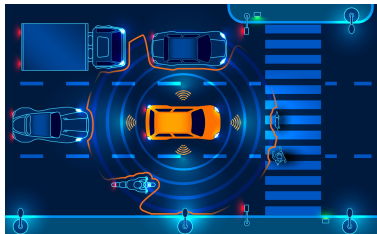
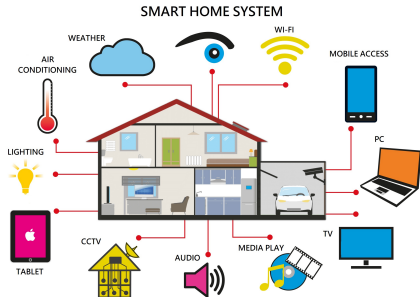
April 7, COOP 2024



About Me

- ▶ Since 2021, PostDoc in Computer Science, LMU Munich
- ▶ 2021, Ph.D. in Electronics Engineering, NTU, Taipei

Modern Computing Systems



*Images from the Internet

Heterogeneous Components

- ▶ Hardware VLSI circuits
- ▶ Software programs
- ▶ Cyber-physical devices

Challenges of Analyzing Heterogeneous Systems

- ▶ Complex interactions
- ▶ Distributed computing
- ▶ Modeling difficulties

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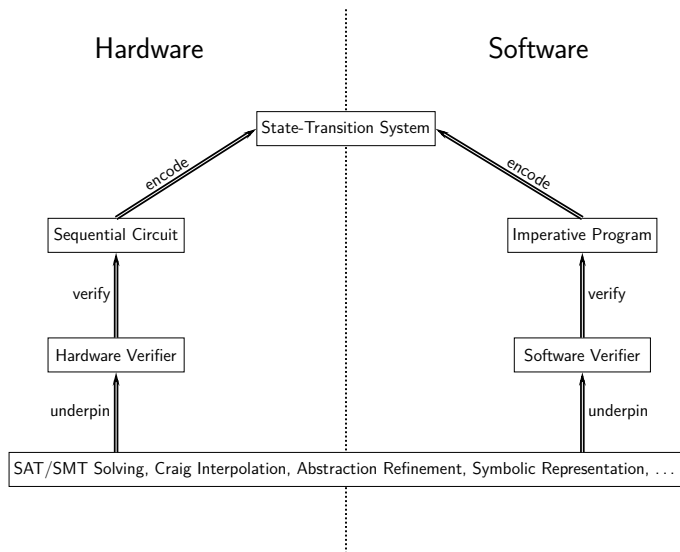
Cooperative and cross-disciplinary approaches are necessary.

Challenges of Analyzing Heterogeneous Systems

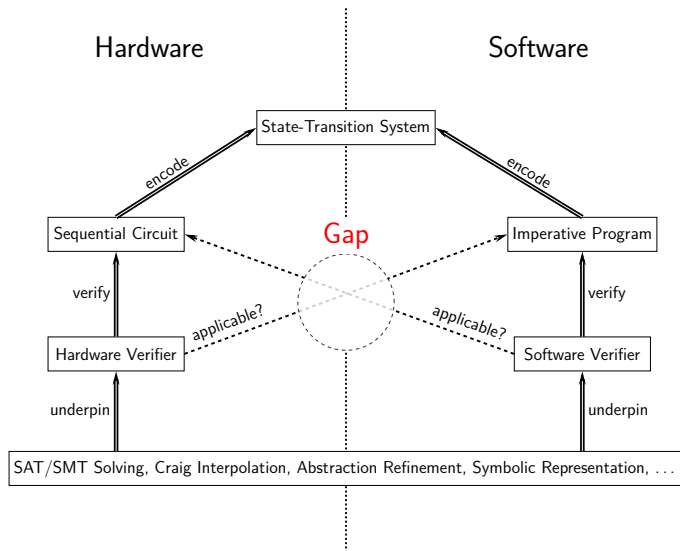
- ▶ Complex interactions
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- ▶ ...

Cooperative and cross-disciplinary approaches are necessary. We should leverage all available knowledge (from other research communities) to improve the state of the art!

Conventional HW and SW Formal Verification



Conventional HW and SW Formal Verification



Bridging HW and SW Analysis

- ▶ Cross-application of each other's advancements
- ▶ Consolidation of formal-verification knowledge

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Software verifiers can detect bugs that hardware verifiers overlook.
Hardware-verification algorithms can improve software verifiers.

Bridging HW and SW Analysis

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- ▶ Consolidation of formal-verification knowledge

Software verifiers can detect bugs that hardware verifiers overlook.
Hardware-verification algorithms can improve software verifiers.

- ▶ Join forces for heterogeneous systems

Agenda

1. Cross-application of HW and SW formal verification
 - 1.1 Applying SW analyzers to HW verification tasks
 - 1.2 Applying HW model checkers to SW verification tasks

2. Knowledge consolidation of formal verification
 - 2.1 Transferability of HW algorithms to SW verification

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Cross-Application of HW and SW Techniques

- ▶ Applying SW analyzers to HW verification tasks
 - ▶ Publications at TACAS 2023 and 2024 [1, 2]
- ▶ Applying HW model checkers to SW verification tasks
 - ▶ CPV: a new circuit-based verifier in SV-COMP 2024 [3]
- ▶ Adopting HW algorithms to verify programs
 - ▶ Publication in *Journal of Automated Reasoning* [4]

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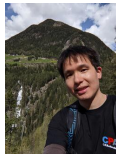
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Bridging Hardware and Software Analysis with Btor2C: A Word-Level-Circuit-to-C Translator

Dirk Beyer, Po-Chun Chien, and Nian-Ze Lee

LMU Munich, Germany

Published at the 29th International Conference on
Tools and Algorithms for the Construction and Analysis of Systems (TACAS), 2023



Research Questions

- ▶ Evaluating SW analyzers on HW verification tasks
- ▶ Complementing HW verification with SW analyzers

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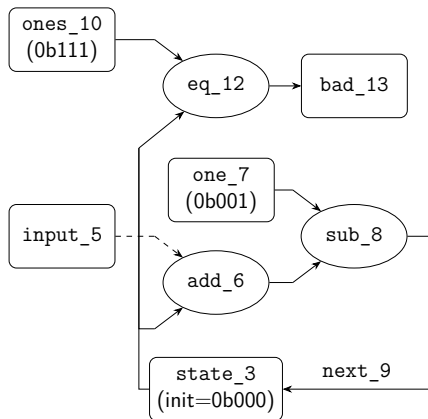
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43 HW-verification tasks uniquely solved by SW analyzers in our evaluation → enhance HW quality assurance

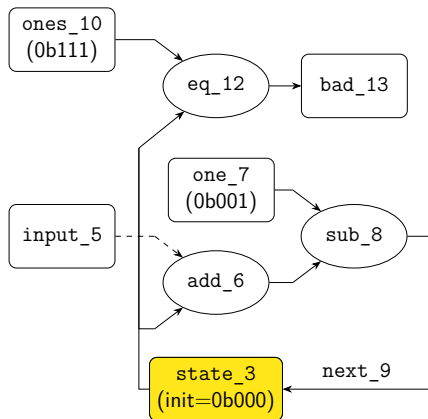
The BTOR2 Language

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2 zero 1
3 state 1
4 init 1 3 2
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8 sub 1 6 7
9 next 1 3 8
10 ones 1
11 sort bitvec 1
12 eq 11 3 10
13 bad 12
```



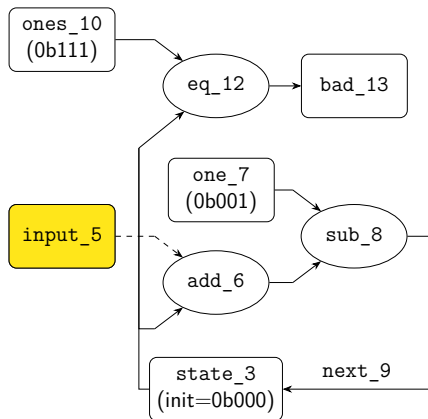
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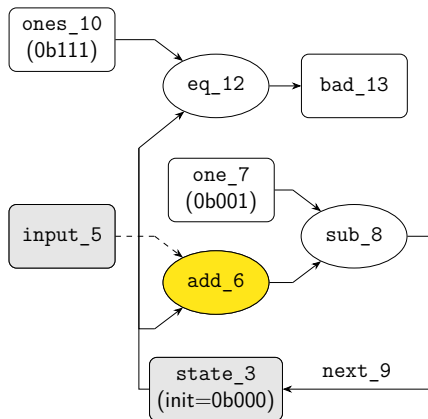
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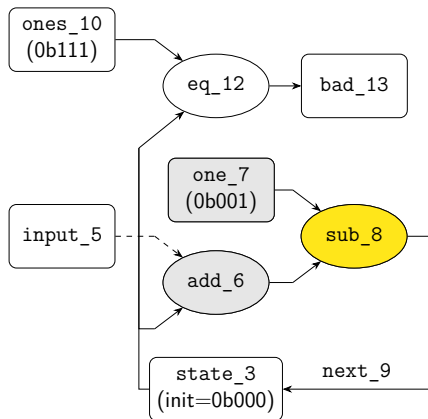
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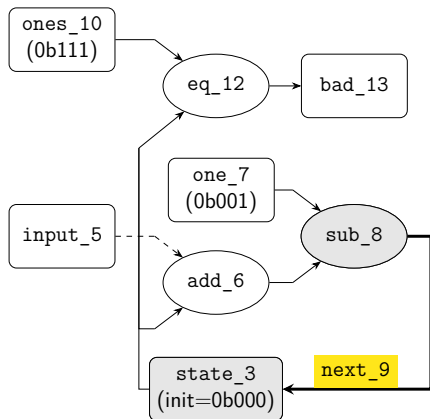
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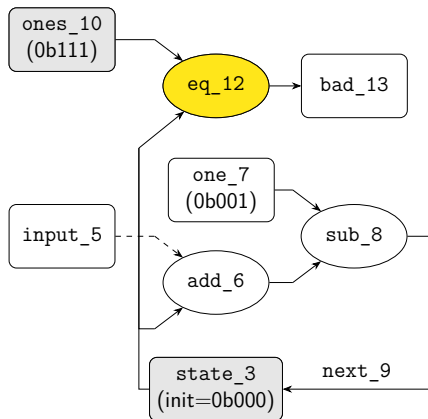
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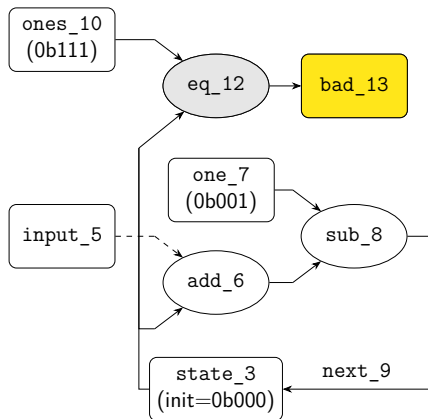
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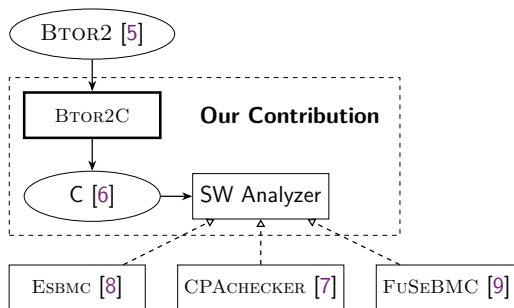


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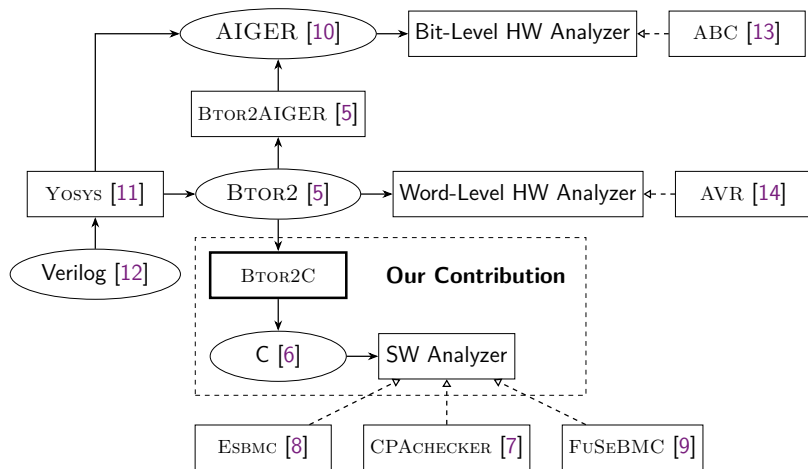
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Our Contribution



Our Contribution



Translating BTOR2 to C

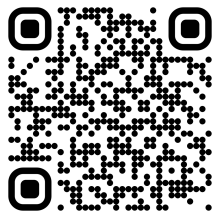
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1 void main() {
2     typedef unsigned char SORT_1;
3     typedef unsigned char SORT_11;
4     const SORT_1 var_2 = 0b000;
5     const SORT_1 var_7 = 0b001;
6     const SORT_1 var_10 = 0b111;
7     SORT_1 state_3 = var_2;
8     for (;;) {
9         SORT_1 input_5 = nondet_uchar();
10        input_5 = input_5 & 0b111;
11        SORT_11 var_12 = state_3 == var_10;
12        SORT_11 bad_13 = var_12;
13        if (bad_13) { ERROR: abort(); }
14        SORT_1 var_6 = state_3 + input_5;
15        var_6 = var_6 & 0b111;
16        SORT_1 var_8 = var_6 - var_7;
17        var_8 = var_8 & 0b111;
18        state_3 = var_8;
19    }
20 }
```

BTOR2C: Btor2-to-C Translator

- ▶ A lightweight tool
 - ▶ Written in C++ with ~ 2 K LOC
 - ▶ Use the frontend parser provided by BTOR2TOOLS [17]
- ▶ Open-source under Apache License 2.0

<https://gitlab.com/sosy-lab/software/btor2c>



Evaluation

On 1 008 safe and 490 unsafe BTOR2 verification tasks:

- ▶ **RQ1:** How do SW analyzers perform on HW tasks?
Quite decent! Each analyzer showcases different strength
- ▶ **RQ2:** Can SW analyzers complement HW model checkers?
*Yes, **43** tasks were uniquely solved by SW verifiers*

Overall Results

Tool	ABC	AVR	CPACHECKER	ESBMC	VERIABS
Algorithm	PDR	PDR	PA	KI	LA
Input	AIGER	BTOR2	C (bit-masking applied lazily)		
Correct results	862	736	280	410	393
BV proofs	524	458	189	93	49
BV alarms	338	233	91	315	342
Array proofs	–	45	0	0	0
Array alarms	–	0	0	2	2

Summary

- ▶ BTOR2C: BTOR2 circuits to C programs
 - ▶ Applying off-the-shelf software analyzers to hardware
 - ▶ Improving quality assurance for hardware
- ▶ **43** tasks uniquely solved by software verifiers
- ▶ The reproduction artifact [23] is available via Zenodo.



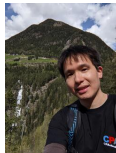
Btor2-Cert: A Certifying Hardware-Verification Framework Using Software Analyzers

Zsófia Ádám^{1,2}, Dirk Beyer², Po-Chun Chien²,
Nian-Ze Lee², and Nils Sirrenberg²

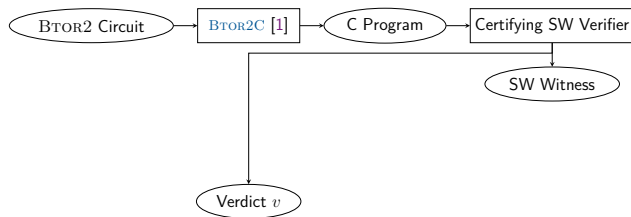
¹Budapest University of Technology and Economics, Hungary

²LMU Munich, Germany

TACAS 2024-04-11

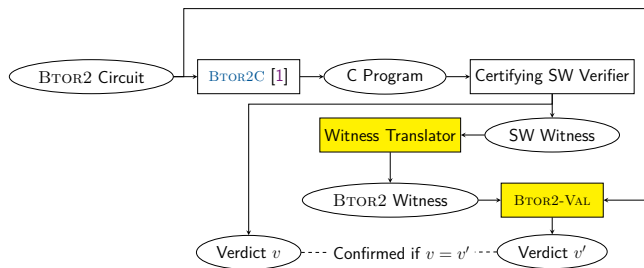


Certifying Verification for BTOR2 with SV Tools



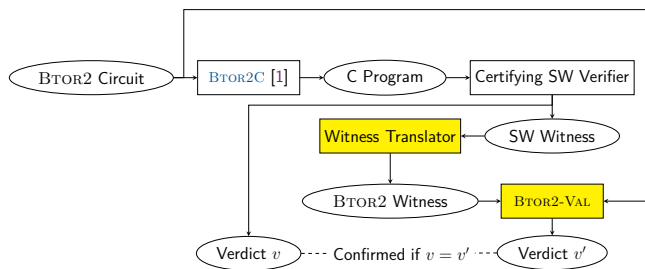
- ▶ BTOR2 [5] word-level circuits and translator BTOR2C [1]
- ▶ Software verifiers in SV-COMP [24]

Certifying Verification for BTOR2 with SV Tools



- ▶ BTOR2 [5] word-level circuits and translator BTOR2C [1]
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- ▶ SW-to-HW witness translation and BTOR2-VAL

Certifying Verification for BTOR2 with SV Tools



- ▶ BTOR2 [5] word-level circuits and translator BTOR2C [1]
- ▶ Software verifiers in SV-COMP [24]
- ▶ SW-to-HW witness translation and BTOR2-VAL
- ▶ On 1214 BTOR2 circuits, BTOR2-CERT
 - ▶ found missed bugs by CBMC [25] to complement ABC [13]
 - ▶ derived invariants by CPACHECKER [7] to accelerate ABC

Agenda

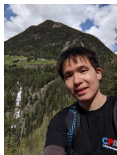
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CPV: A Circuit-Based Program Verifier

Po-Chun Chien and Nian-Ze Lee

LMU Munich, Germany

First-Time Participant at SV-COMP 2024 (April 8)



Research Question

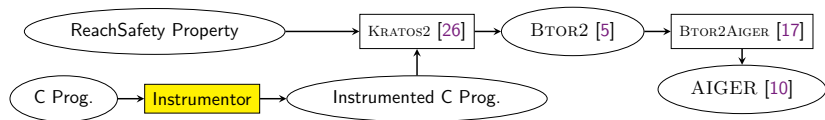
- ▶ **Sequential circuit** as an alternative intermediate representation for program analysis
 - ▶ Leveraging HW model checking as backend

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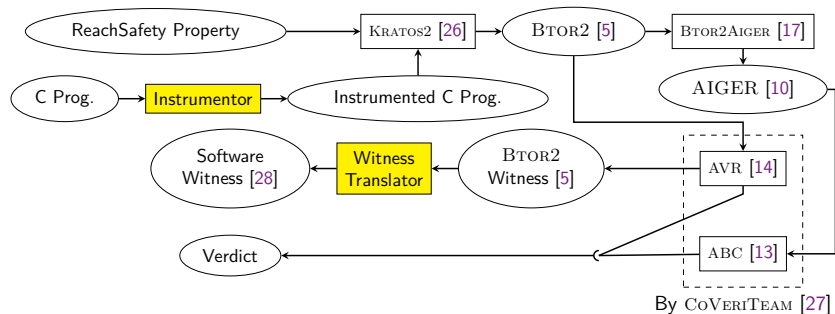
CPV ranks 6th out of 26 in *ReachSafety* as a first-time participant in SV-COMP 2024!

Software Architecture of CPV



- ▶ Program instrumentation for retrieving witness information

Software Architecture of CPV



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- ▶ HW-to-SW witness translation

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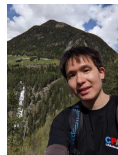
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A Transferability Study of Interpolation-Based Hardware Model Checking to Software Verification

Dirk Beyer, Po-Chun Chien, Marek Jankola, and Nian-Ze Lee

LMU Munich, Germany



Research Question

- ▶ Can research conclusions from hardware model checking be transferred to software verification?

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Characteristics of two interpolation-based algorithms [30, 31] for hardware are shown to be transferrable to software.

Transferring HV Studies to SV Contexts

- ▶ Implement two hardware-verification algorithms in CPACHECKER and evaluate on ~ 9 K software tasks
 - ▶ Baseline: IMC [32] (McMillan, 2003) (software adoption to appear in *JAR* [4])

Transferring HV Studies to SV Contexts

- ▶ Implement two hardware-verification algorithms in `CPACHECKER` and evaluate on ~ 9 K software tasks
 - ▶ Baseline: IMC [32] (McMillan, 2003) (software adoption to appear in *JAR* [4])
- ▶ Interpolation-Sequence-Based Model Checking, 2009 [30]
 - ▶ Benchmark set: 136 tasks derived from industrial designs
 - ▶ Claims
 - ▶ Faster than IMC on unsafe tasks (✓)
 - ▶ Faster than IMC on safe tasks if higher unrolling (?)
 - ▶ Overall, faster than IMC (by 30%) (?)

Transferring HV Studies to SV Contexts

- ▶ Implement two hardware-verification algorithms in CPACHECKER and evaluate on ~ 9 K software tasks
 - ▶ Baseline: IMC [32] (McMillan, 2003) (software adoption to appear in JAR [4])
- ▶ Interpolation-Sequence-Based Model Checking, 2009 [30]
- ▶ Intertwined Forward-Backward Reachability Analysis Using Interpolants, 2013 [31]
 - ▶ Benchmark set: 37 tasks derived from industrial designs
 - ▶ Claims
 - ▶ Local strengthening enough to refute spurious bugs (✓)
 - ▶ Faster than IMC on safe tasks (?)
 - ▶ Computes more interpolants than IMC (✓)
 - ▶ More sensitive to the sizes of interpolants (?)
 - ▶ Overall, faster than IMC (by 36%) (?)

Summary

- ▶ Transferability of algorithmic characteristics confirmed
 - ▶ Interpolation-sequence faster to find bugs
 - ▶ Local strengthening enough to refute spurious bugs
- ▶ Unified knowledge across hardware and software for full-stack system verification

Agenda

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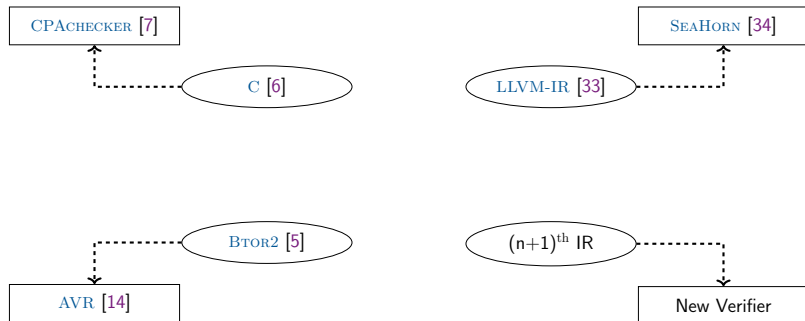
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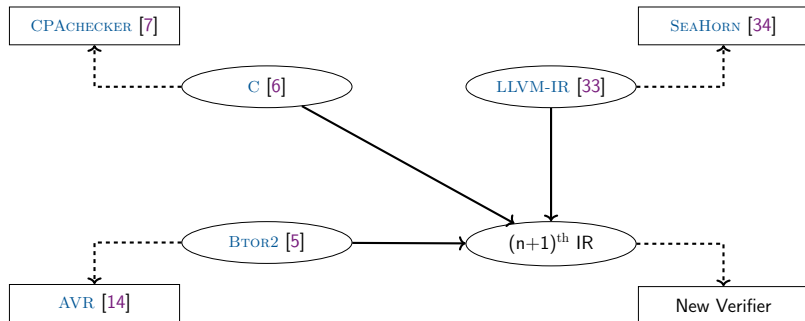
Bridging HW and SW Analysis: So Far

- ▶ SW tools uniquely solving HW tasks [1, 2]
- ▶ HV algorithms [4] and tools [3] improving SV
- ▶ Transferability of algorithmic characteristics [29]

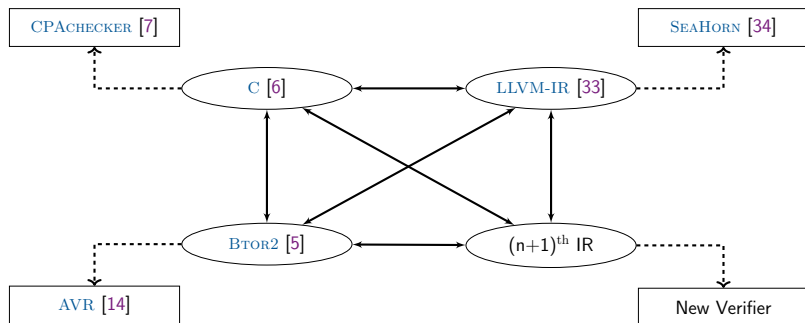
Critical Reflection



Critical Reflection



Critical Reflection



Transformation between different representations to leverage their unique strengths

Challenges of Heterogeneous Systems

- ▶ Firmware
 - ▶ Ex: data privacy of smart devices
 - ▶ Specific constructs (e.g., assembly), hardware modeling
 - ▶ Current practices: manual review or testing
 - ▶ **Idea**: circuit-based program verification

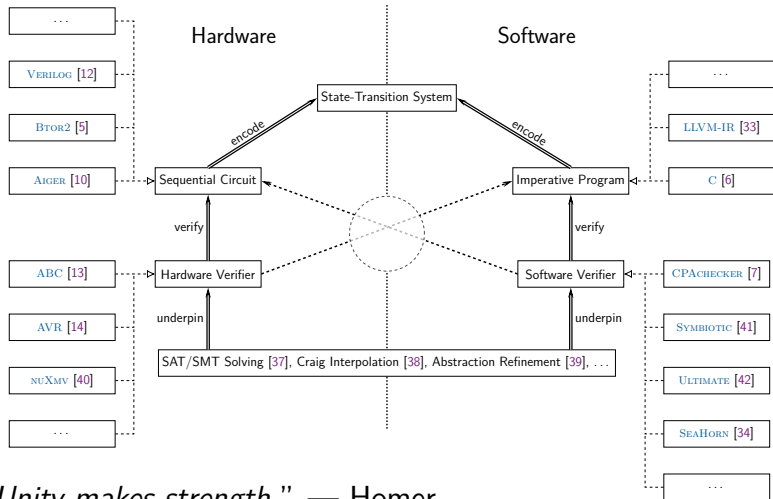
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- ▶ Neural networks
 - ▶ Ex: autonomous driving
 - ▶ Mathematical operations
 - ▶ Current practices: mostly on models (cf. [VNN-COMP](#))
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 - ▶ **Idea**: verification of arithmetic circuits

Challenges of Heterogeneous Systems

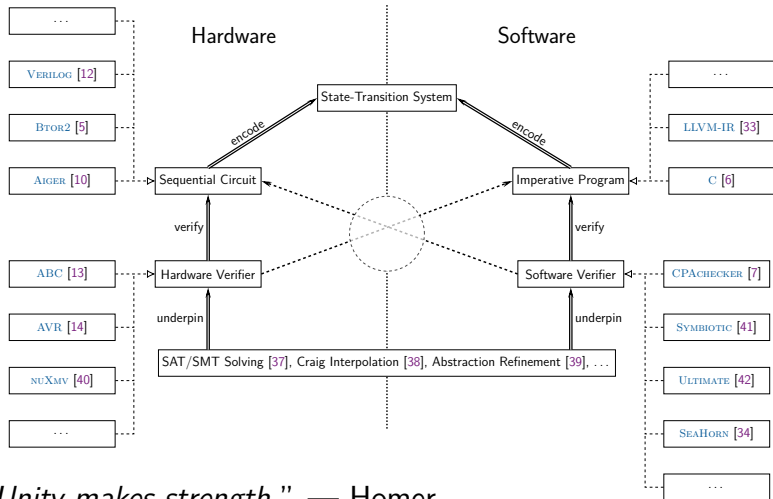
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 - ▶ Less on C implementations (e.g., [NeuroCodeBench](#) [35])
 - ▶ **Idea**: verification of arithmetic circuits
- ▶ Hardware/software co-design (embedded systems)
 - ▶ Current practices: lower level verification conditions [36]
 - ▶ **Idea**: on-the-fly translation and abstraction as HW or SW

Closing the Gap between HW and SW Analysis



"Unity makes strength." — Homer

Closing the Gap between HW and SW Analysis



"Unity makes strength." — Homer

We are hiring! (A full Ph.D. position funded by DFG)

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