CPV: A Circuit-Based Program Verifier

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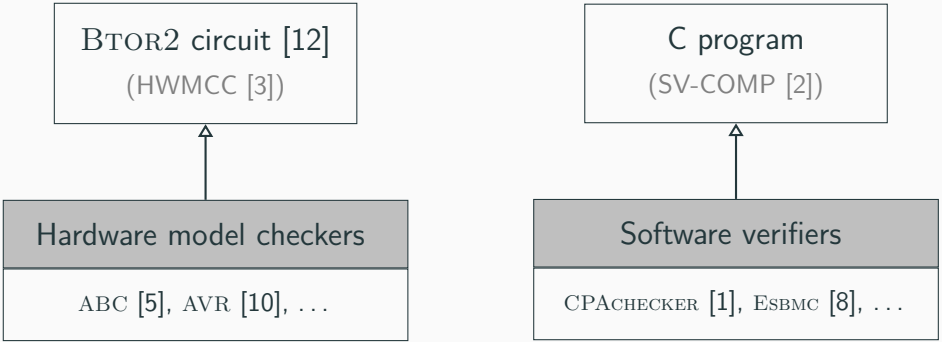
SV-COMP 2025 @ Hamilton, Canada

Motivation

BTOR2 circuit [12]
(HWMCC [3])

C program
(SV-COMP [2])

Motivation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(HWMCC [3])
C program
(SV-COMP [2])
Hardware model checkers
ABC [5], AVR [10], . . .
Software verifiers
CPAchecker [1], Esbmc [8], . . .

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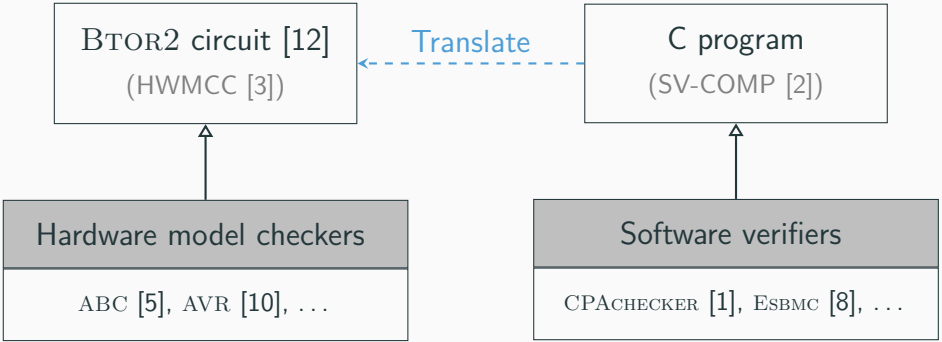
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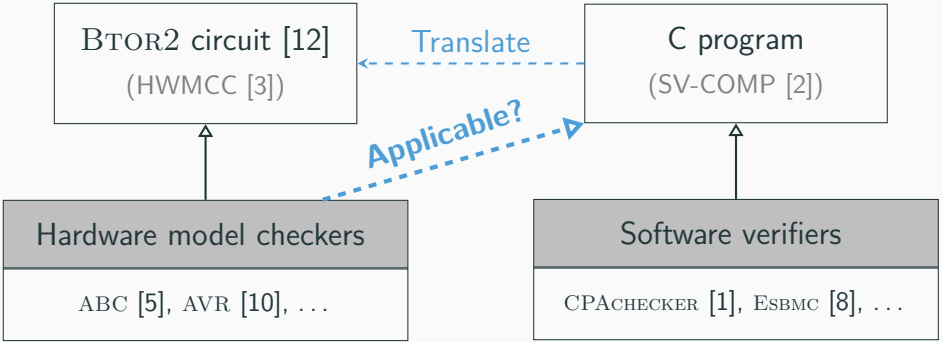
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Applicable?
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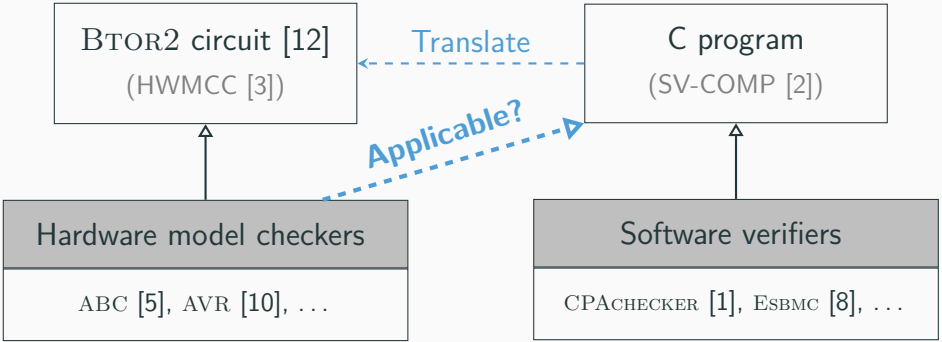
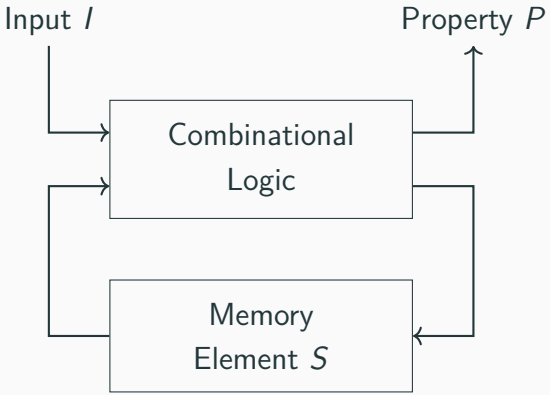


Could circuits serve as IR for program verification?

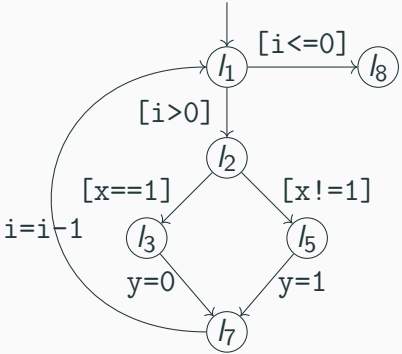
Hardware Model: Sequential Circuit



- State transition:
  $S' \leftarrow T_{func}(S, I)$
- Property:
  $P(S)$ or $P(S, I)$

Large-Block Encoding

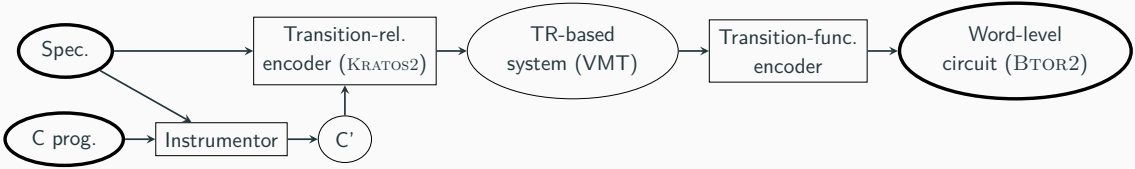
C Program → Transition Relation



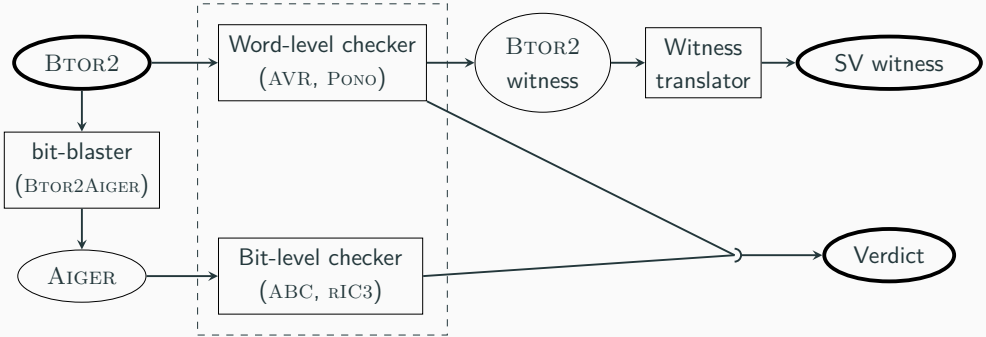
Each loop-free section as a block:

$$
\begin{aligned}
TR = (&pc = l_1 \wedge pc' = l_1 \wedge i > 0 \\
&\wedge i' = i - 1 \wedge y' = ite(x = 1, 0, 1) \ldots) \\
\vee\, (&pc = l_1 \wedge pc' = l_8 \wedge i \leq 0 \wedge i' = i \ldots) \\
\vee\, &\ldots
\end{aligned}
$$

System Architecure: Frontend



System Architecure: Backend

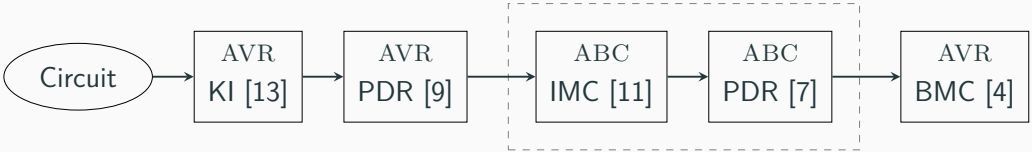


Managed by COVERITEAM

Strategy for SV-COMP

A sequential portfolio consisting of

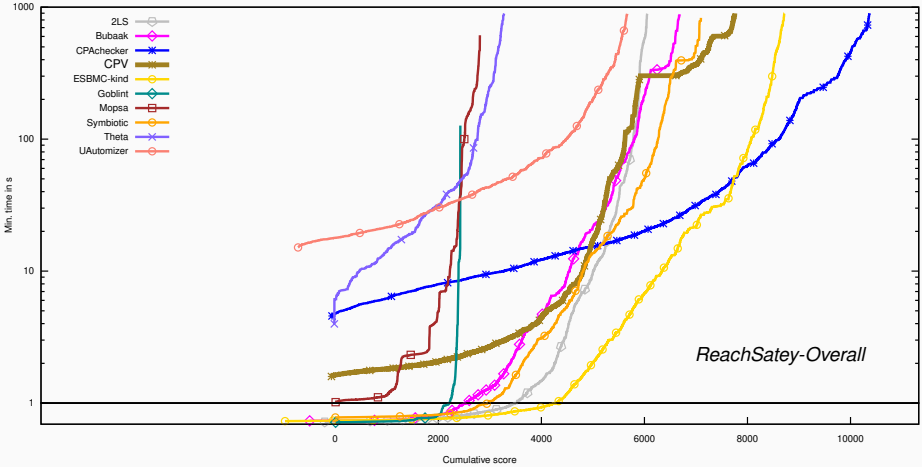
- Different encodings: functional and relational
- Different model-checking engines:



if BTOR2-to-AIGER translation succeeds

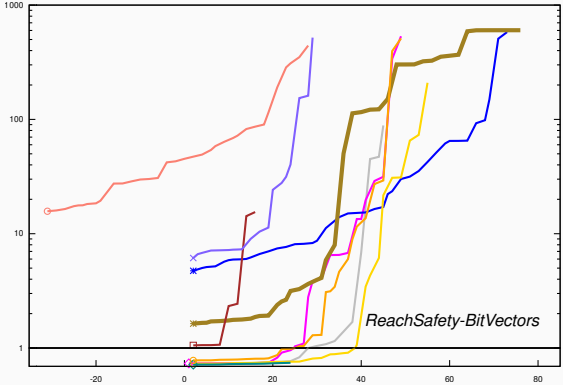
Results in SV-COMP

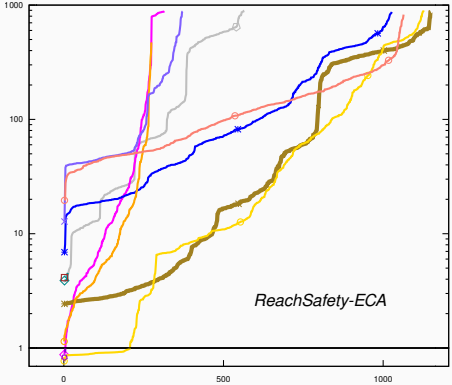
3rd place in *ReachSafety* category (2×, 2×, and 2× in subcategories)



Results in SV-COMP

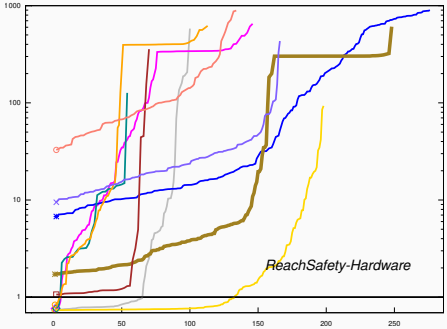
🥇 **1st** place in *ReachSafety-BitVectors* and *-ECA*

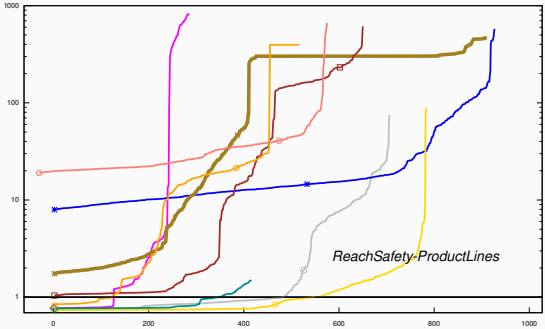




Results in SV-COMP

- **2nd** place in *ReachSafety-Hardware* and *-ProductLines*





Conclusion

- Our verifier CPV [6]
  - encodes programs into circuits and
  - employs hardware model checkers as backend.
- Pretty good performance in SV-COMP!
- Ongoing development:
  - Support termination analysis
  - Integrate more backends from HWMCC

gitlab.com/sosy-lab/software/cpv

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