The Transformation Game: Joining Forces for Verification

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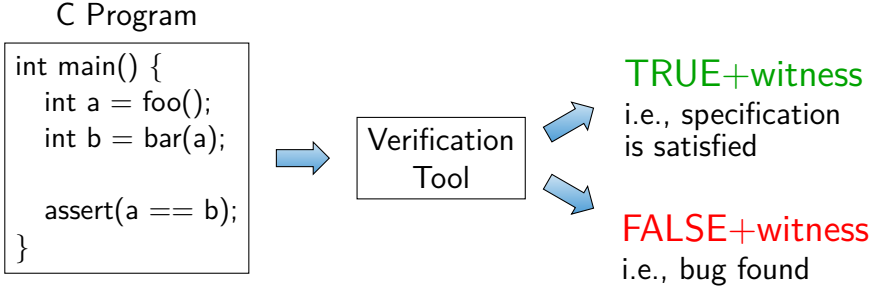
Background of this presentation: Automatic Software Verification



Status on Software Verifiers

- From lack of verifiers to plentitude
- 76 verification tools publicly available [41]
- SV-COMP 2025: 62 verification tools and 18 witness validation tools

Competitions in Software Verification and Testing

Mature research area, and there are tool competitions (alphabetic order):

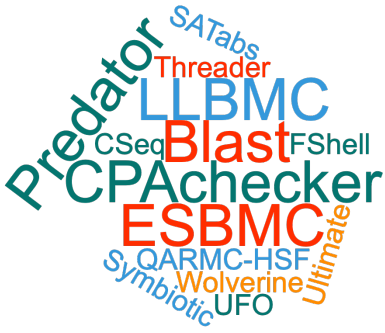
- RERS: off-site, tools, free-style [57]
- SV-COMP: off-site, automatic tools, controlled [10]
- Test-Comp: off-site, automatic tools, controlled [11]
- VerifyThis: on-site, interactive, teams [58]

Broader in formal methods:

- MCC [3]
- SAT-COMP [8]
- SMT-COMP [9]
- TPTP [70]
- HWMCC [43]

SV-COMP (Automatic Tools 2012)

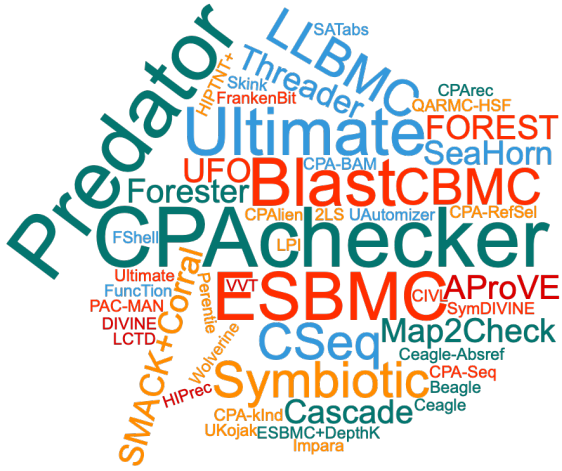
SV-COMP (Automatic Tools 2013, cumulative)



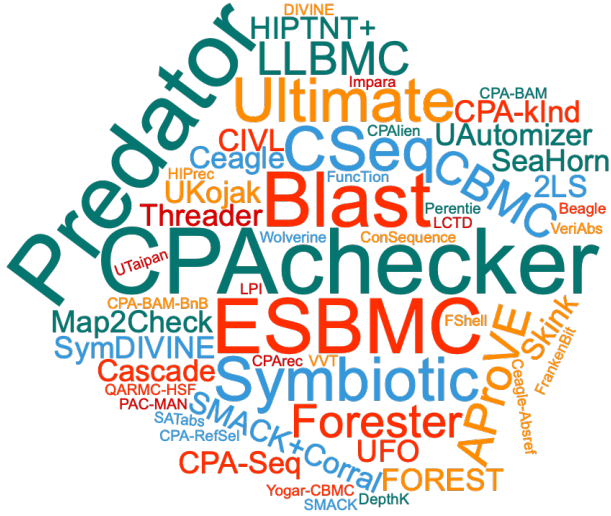
SV-COMP (Automatic Tools 2014, cumulative)

SV-COMP (Automatic Tools 2015, cumulative)

SV-COMP (Automatic Tools 2016, cumulative)

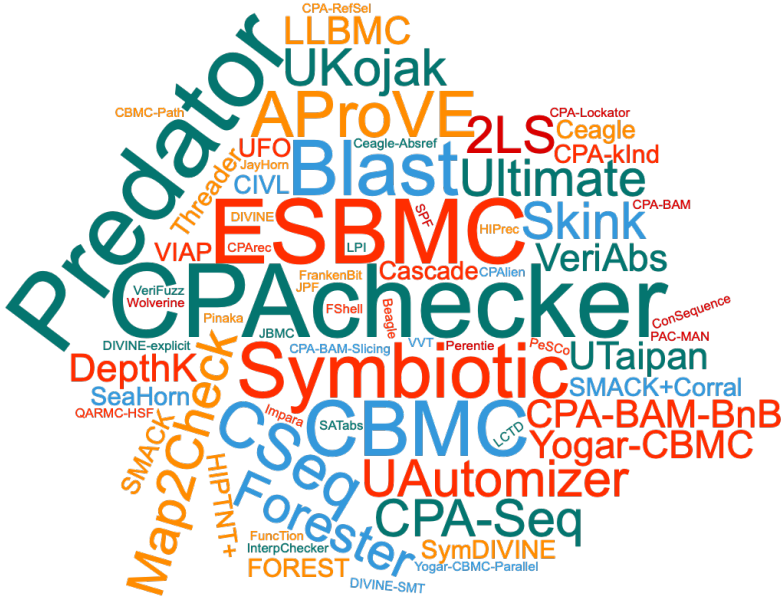


SV-COMP (Automatic Tools 2017, cumulative)

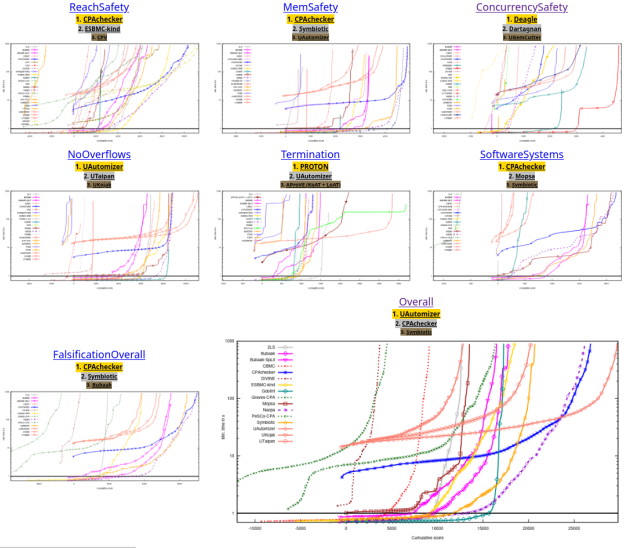


SV-COMP (Automatic Tools 2018, cumulative)

SV-COMP (Automatic Tools 2019, cumulative)



Different Strengths



https://sv-comp.sosy-lab.org/2025/results

Different Techniques (Extract from Report)

Table 8: Algorithms and techniques used by the participating tools; ⌀ for inactive, meta for meta verifiers, and new for first-time participants

Tool	CEGAR	Predicate Abstraction	Symbolic Execution	Bounded Model Checking	k-Induction	Property-Directed Reach.	Explicit-Value Analysis	Numeric. Interval Analysis	Shape Analysis	Separation Logic	Bit-Precise Analysis	ARG-Based Analysis	Lazy Abstraction	Interpolation	Automata-Based Analysis	Concurrency Support	Ranking Functions	Evolutionary Algorithms	Algorithm Selection	Portfolio	Task Translation
2LS				✓	✓			✓	✓		✓						✓				
AISE			✓																		
APROVE																	✓				
BRICK	✓		✓	✓				✓								✓					
BUBAAK			✓								✓					✓	✓			✓	
BUBAAK-SPLIT			✓		✓						✓				✓	✓	✓		✓	✓	
CBMC⌀				✓							✓					✓					
COASTAL⌀			✓																		
CONCURRENTW2T																✓					
COOPERACE meta new																✓			✓	✓	
CPACHECKER	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓		✓	✓	
CPALOCKATOR⌀	✓	✓					✓				✓	✓	✓	✓		✓					
CPA-BAM-BNB⌀	✓	✓					✓				✓	✓	✓	✓							
CPA-BAM-SMG⌀																					
CPA-W2T⌀						✓						✓			✓						
CPROVER-W2T⌀				✓																	
CPV	✓	✓		✓	✓	✓					✓			✓					✓	✓	✓
CRUX⌀			✓																		
CSEQ⌀				✓							✓					✓					

(continues on next page)

Competition Report [38]
https://doi.org/10.1007/978-3-031-90660-2_9

Example CPAchecker [29]: Many Concepts

- Included Concepts:
  - CEGAR [49] Interpolation [33, 21]
  - Configurable Program Analysis [24, 25]
  - Adjustable-block encoding [30]
  - Conditional model checking [23]
  - Verification witnesses [19, 17]
  - Various abstract domains: predicates, intervals, BDDs, octagons, explicit values
- Available analyses approaches:
  - Predicate abstraction [15, 30, 25, 34]
  - Impact algorithm [65, 40, 21]
  - Bounded model checking [50, 21]
  - k-Induction [20, 21]
  - IC3/Property-directed reachability [16]
  - Explicit-state model checking [33]
  - Interpolation-based model checking [31]

Insights from Software Model Checking

- Verifiers have different strengths
- There are plenty of tools
- $\Rightarrow$ Combination of Verification Approaches

Cooperative Verification — Think big!

- Introduce a new level!
- Current tools should become "low level" components (engines)
- Construct combinations
- Clear Interfaces
  via, e.g., Conditions, Witnesses, Test Suites
- Success: SAT, SMT (common interfaces, usable as libraries)
- See also: Little Engines [69], Evidential Tool Bus [51]

Verification by Transformations

Vision: Modular Transformation Paradigm

- Standalone and reusable transformers to construct verifiers
- Well-defined interfaces and exchange formats
- Construction recipes: easy to build new verifiers for different applications

Inputs and Outputs of Transformers: Artifacts

Type	Notation	Usage
Model	$\mathcal{M}$	Description of the system under verification
Specification	Φ	Expected behavior of the system under verification
Verdict	$\mathcal{R}$	Decision on whether a model satisfies a specification
Witness	Ω	Certificate explaining the verdict of a tool
Verification condition	$\mathcal{VC}$	Set of constraints that encode the behavior of a model

Example Transformers

Type	Signature	Functionality
Translator	$\mathcal{M} \mapsto \mathcal{M}$	Translates a model to a behaviorally equivalent one in a different language
Encoder	$\mathcal{M} \mapsto \mathcal{VC}$	Describes partial or complete behavior of a model as a verification condition
Specification transformer	$\mathcal{M} \times \Phi \mapsto \mathcal{M} \times \Phi$	Converts a verification task to an equisatisfiable one with a different specification
Witness transformer	$\mathcal{M} \times \Omega \mapsto \Omega$	Transforms a witness for a model to another witness, e.g., by making it more precise
Pruner	$\mathcal{M} \times \Omega \mapsto \mathcal{M}$	Removes irrelevant or fully-explored parts of a model based on a witness

Literature

The Transformation Game: Joining Forces for Verification, Festschrift 60th Birthday Jost-Pieter Katoen, 2024, available at doi:10.1007/978-3-031-75778-5_9

Application Examples

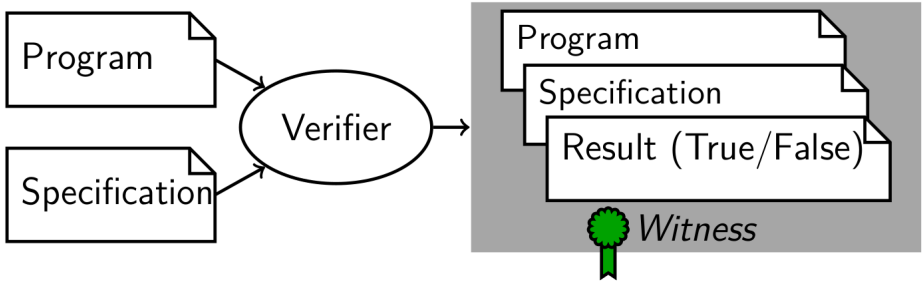
- (A1) Verification Witnesses and Validation
- (A2) LIV: Decomposing Validator
- (A3) CoVeriTeam: Language and Tool for Combination
- (A4) Simple Combinations
- (A5) Btor2C: Transforming from Hardware to Software
- (A6) Certifying Verification for BTOR2 with SV Tools
- (A7) Transformation-Based Verification with MoXI

Application Examples

- (A8) Transformation of Specifications
- (A9) Conditional Model Checking (CMC)
- (A10) Reducer-Based CMC
- (A11) Modularization of CEGAR
- (A12) Combining Interactive and Automatic Methods
- (A13) Loop Abstraction

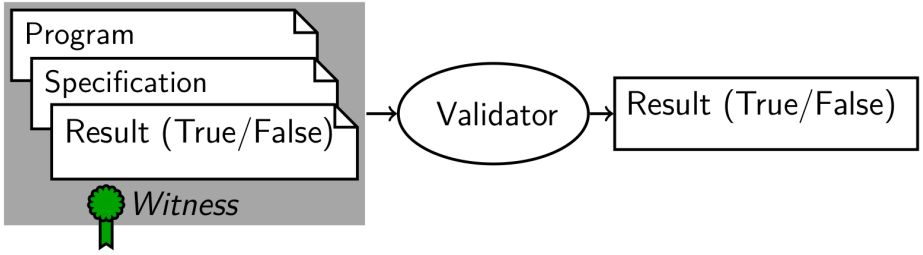
(A1) Software Verification with Witnesses

Witnesses are an important interface between tools.



[19, Proc. FSE 2015] [17, Proc. FSE 2016] [18, TOSEM 2022]

(A1) Witness-Based Result Validation



- Validate untrusted results
- Reestablish proof of correctness or violation
- Easier than full verification

(A1) Verification and Validation

Given program P and specification φ

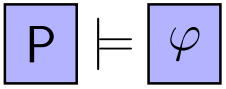
- Verification: **prove** that $P \models \varphi$
  (mainly invariant construction)
- Validation with witness w: **re-prove** that $P \models \varphi$

AI can be used to

- **write** programs
- **suggest** invariants for programs

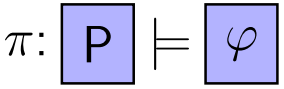
(A1) Correctness Witnesses

Program P, specification φ, proof π



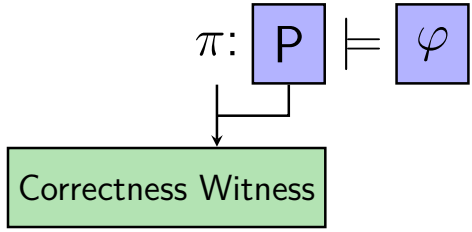
(A1) Correctness Witnesses

Program P, specification φ, proof π



(A1) Correctness Witnesses

Program P, specification φ, proof π



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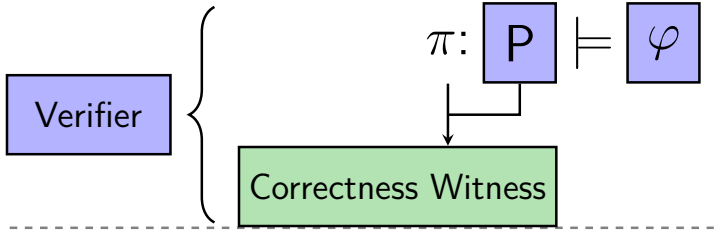
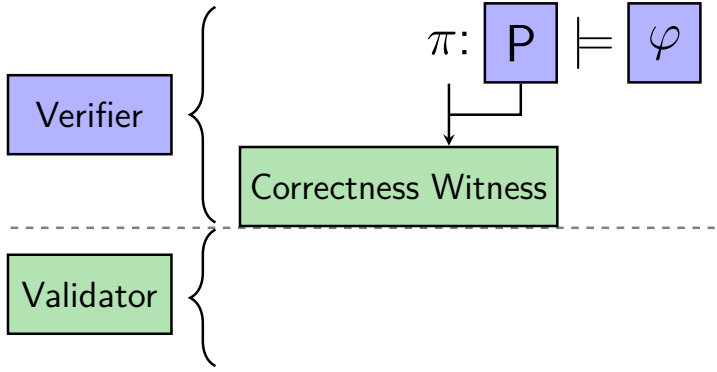
Program P, specification φ, proof π



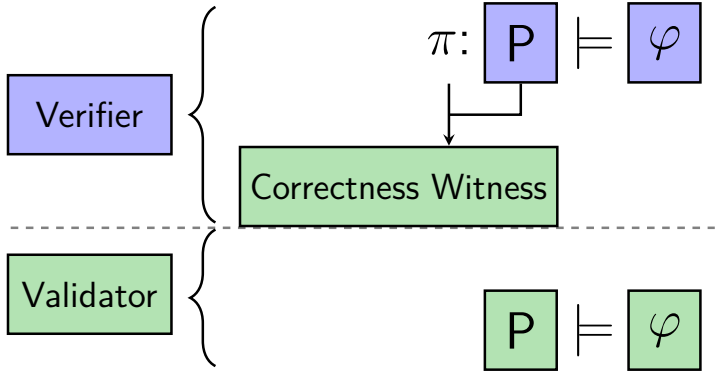
(A1) Correctness Witnesses

Program P, specification φ, proof π



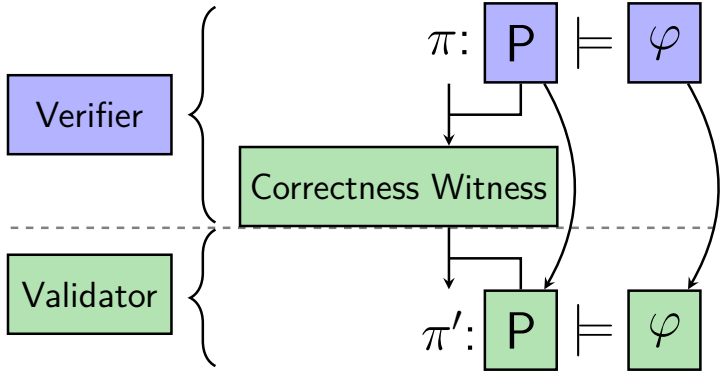
(A1) Correctness Witnesses

Program P, specification φ, proof π



(A1) Correctness Witnesses

Program P, specification φ, proof π



(A1) Example Program and Witness

Program:

```
int main() {
  unsigned char n = __nondet_uchar();
  if (n == 0) {
    return 0;
  }
  unsigned char v = 0;
  unsigned int  s = 0;
  unsigned int  i = 0;
  while (i < n) {
    v = __nondet_uchar();
    s += v;
    ++i;
  }
  if (s < v) {
    reach_error();
    return 1;
  }
  if (s > 65025) {
    reach_error();
    return 1;
  }
  return 0;
}
```

Witness (format v2.0):

```
content:
  - invariant:
      type: loop_invariant
      location:
        file_name: "inv-a.c"
        line: 12
        column: 1
        function: main
      value: "s <= i*255 && 0 <= i && i <= 255 && n <= 255"
      format: c_expression
```

(A1) State of the Art

- 18 validators exist for C and Java
- 4 formats for witnesses exist
  (GraphML and YAML, correctness and validation)
- Competition on Software Verification (SV-COMP) has a validation track

Certifying Algorithms [64] are used also in SAT and SMT.

(A2) LIV — Decomposing Validator

[36, Proc. ASE 2023], Idea from A. Appel

Program:

```
1   int x = 0;
2   int sum = 0 ;
3   //@ loop invariant I;
4   while (x<10) {
5     x++;
6     sum+=x;
7   }
8   assert (sum<=55);
```

Proof Obligations:

- $\{P\}s_0\{Inv\}$
- $\{Inv \wedge Cond\}Body\{Inv\}$
- $Inv \Rightarrow Q$

(A2) From Proof Obligations to Straight-Line Programs

Proof Obligations:

- $\{P\}s_0\{Inv\}$ (Base Case)
- $\{Inv \wedge Cond\}Body\{Inv\}$ (Inductiveness)
- $Inv \wedge \neg Cond \Rightarrow Q$ (Safety)

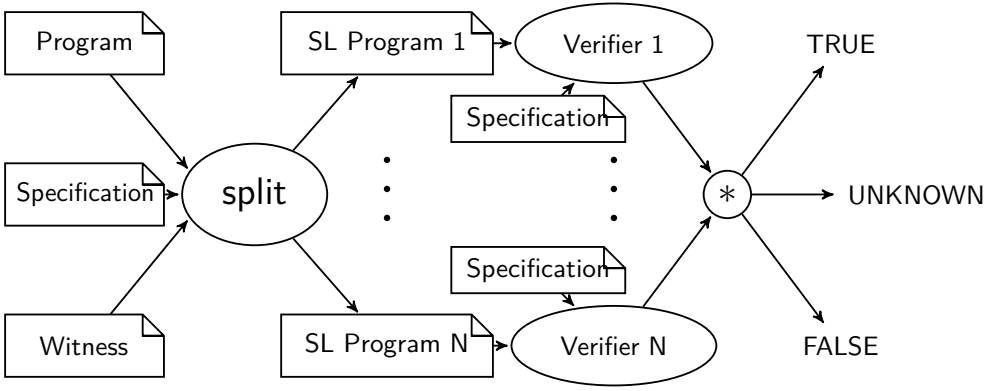
Straight-Line Programs:

```
1  int x = 0;
2  int sum = 0;
3  assert(Inv);
```

```
1  int x = nondet();
2  int sum = nondet();
3  assume(Inv && C);
4  x++;
5  sum += x;
6  assert(Inv);
```

```
1  int x = nondet();
2  int sum = nondet();
3  assume(Inv && ! C);
4  assert(Q);
```

(A2) Workflow of LIV



- Can use any off-the-shelf verifier from SV-COMP as backend
- Small frontend using pycparser for AST-based splitting

(A3) Example Combination (in DSL CoVeriTeam)

CoVeriTeam: Language and Tool [27, Proc. TACAS 2022]

Algorithm Witness Validation [19, 17]

Input: Program p, Specification s
Output: Verdict

```
1: verifier := Verifier("Ultimate Automizer")
2: validator := Validator("CPAchecker")
3: result := verifier.verify(p, s)
4: if result.verdict ∈ {TRUE, FALSE} then
5:     result = validator.validate (p, s, result.witness)
6: return  (result.verdict, result.witness)
```

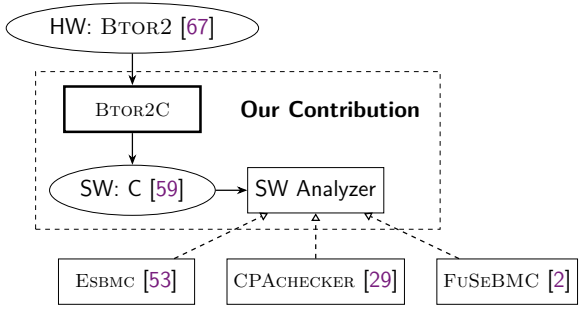
(A4) Simple Combination without Cooperation

Often, even simple combinations help!

Portfolio construction using off-the-shelf
verification tools [28, Proc. FASE 2022]

Consider AWS category (177 tasks) in SV-COMP 2022:
CBMC: 69 (8 wrong)
CoVeriTeam-Parallel-Portfolio: 147 (3 wrong)
(improvement did not require any change in a verification tool)

(A5) Btor2C: Transforming from Hardware to Software



- **43** HW-verification tasks uniquely solved by SW analyzers in our evaluation
  → enhance HW quality assurance using SW analyzers

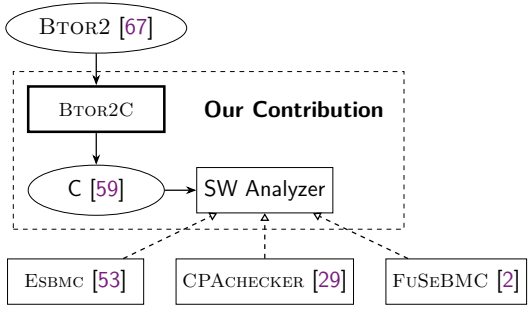
[14, Proc. TACAS '23]

(A5) Btor2C: Btor2-to-C Translator

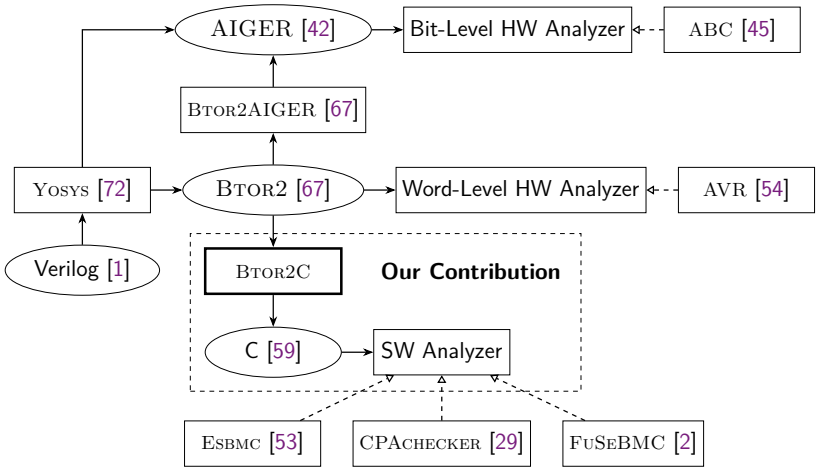
- A lightweight tool
  - Written in C++ with ∼2 K LOC
  - Use the frontend parser provided by Btor2Tools [66]
- Open-source under Apache License 2.0

https://gitlab.com/
sosy-lab/software/btor2c

(A5) Btor2C in Action



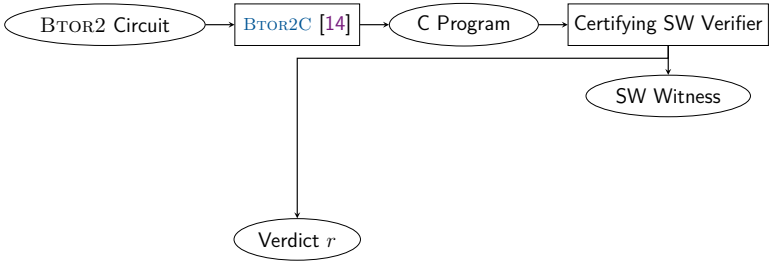
(A5) Btor2C in Action



(A5) Results using BTOR2C

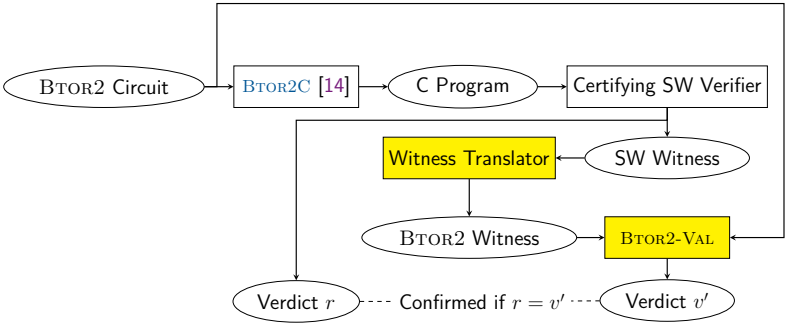
Tool	ABC	AVR	CPACHECKER	ESBMC	VERIABS
Algorithm	PDR	PDR	PA	KI	LA
Input	AIGER	BTOR2	C (bit-masking applied lazily)		
Correct results	**862**	736	280	**410**	393
BV proofs	**524**	458	**189**	93	49
BV alarms	**338**	233	91	315	**342**
Array proofs	–	**45**	0	0	0
Array alarms	–	0	0	**2**	**2**

(A6) Certifying Verification for BTOR2 with SV Tools



- BTOR2 [67] word-level circuits and translator BTOR2C [14]
- Software verifiers in SV-COMP [13]

(A6) Certifying Verification for BTOR2 with SV Tools



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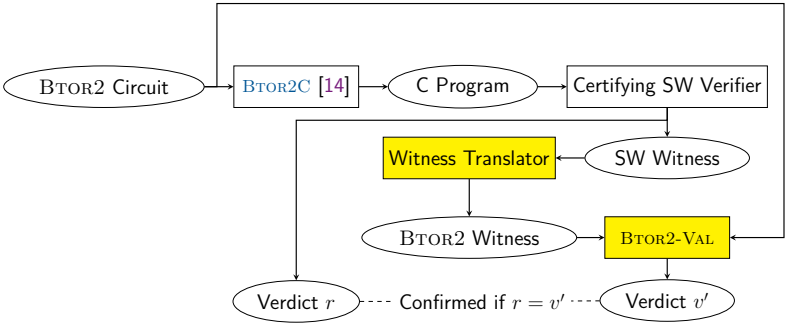
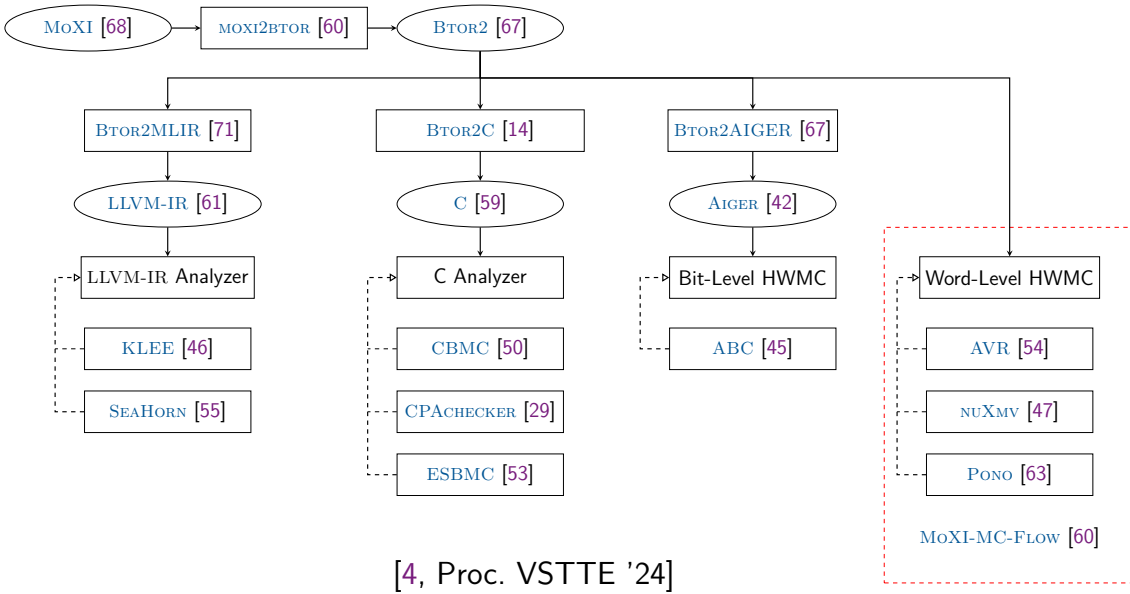
- SW-to-HW witness translation and BTOR2-VAL

(A6) Certifying Verification for BTOR2 with SV Tools



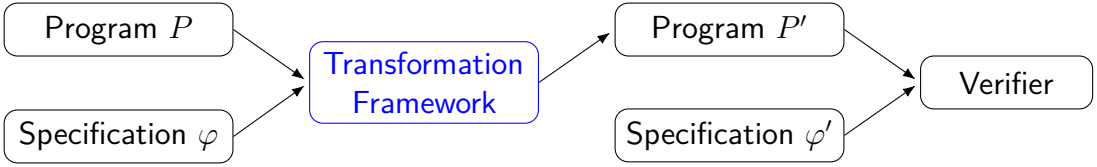
- BTOR2 [67] word-level circuits and translator BTOR2C [14]
- Software verifiers in SV-COMP [13]
- SW-to-HW witness translation and BTOR2-VAL
- On 1214 BTOR2 circuits, BTOR2-CERT achieved that
  - CBMC [50] found 37 bugs that ABC [45] missed
  - derived invariants by CPACHECKER [29] accelerated ABC

(A7) Transformation-Based Verification with MoXI



[4, Proc. VSTTE '24]

(A8) Transformation of Specifications

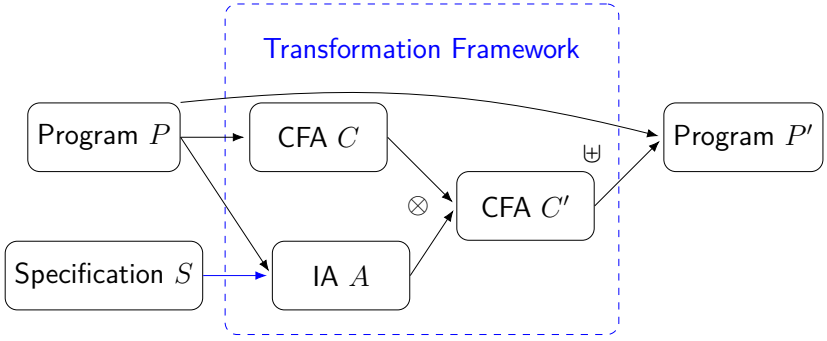


Our framework:

- *Easy to adopt* → Used by three tools in SV-COMP 25
- *Moudular* → Can be used by any verifier supporting SV-COMP syntax
- *Configurable* → The transformations given by *Instrumentation Automata (IA)*

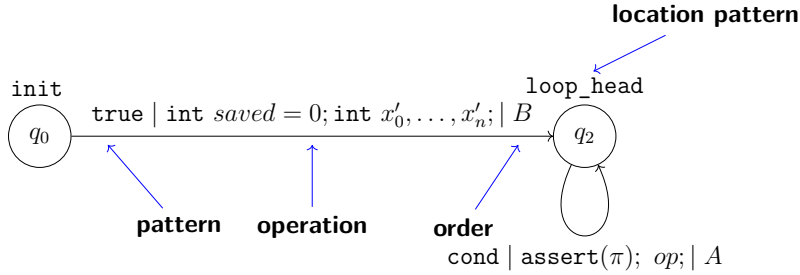
Proc. SPIN 2025

(A8) Transformation of $P \models \varphi$ to $P' \models \varphi'$



- Instrumentation Automaton (IA)
- Sequentialization Operation ($\otimes$)
- Instrumentation Operation ($\uplus$)

(A8) An Instrumentation Automaton for Termination

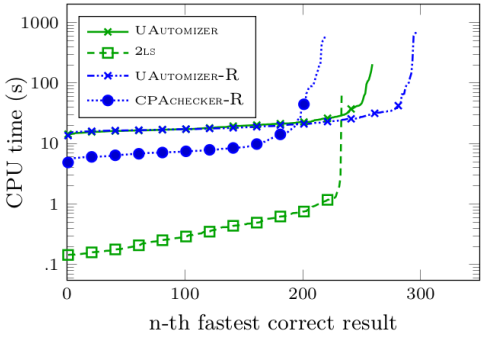


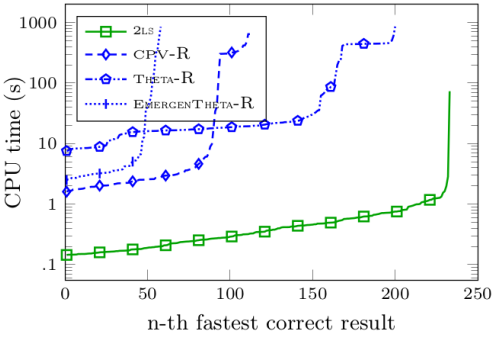
$op \equiv [\texttt{nondet}() \ \wedge \ saved = 0] \ ? \ x'_0 = x_0; \ldots; x'_n = x_n; saved = 1;$
$\pi \equiv (saved = 1) \Rightarrow (x'_0 \neq x_0 \vee x'_1 \neq x_1 \vee \cdots \vee x'_n \neq x_n);$

(A8) Tools and Their Specifications

Tool	reachability	no overflow	memory cleanup	termination
CPAchecker [5]	✓	✓	✓	✓
UAutomizer [56]	✓	✓	✓	✓
UTaipan [52]	✓	✓	✗	✗
2ls [62]	✓	✗	✗	✓
Theta [7]	✓	✗	✗	✗
EmergenTheta [6]	✓	✗	✗	✗
CPV [48]	✓	✗	✗	✗

(A8) Results for Termination → Reachability



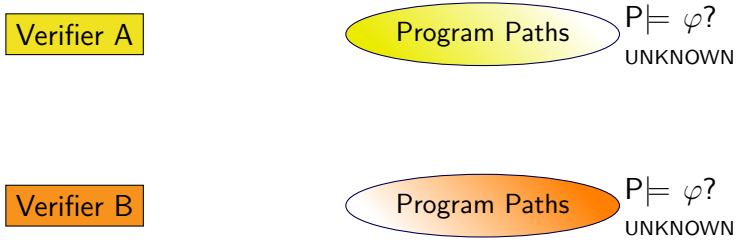


(A8) Results on Termination Reduction

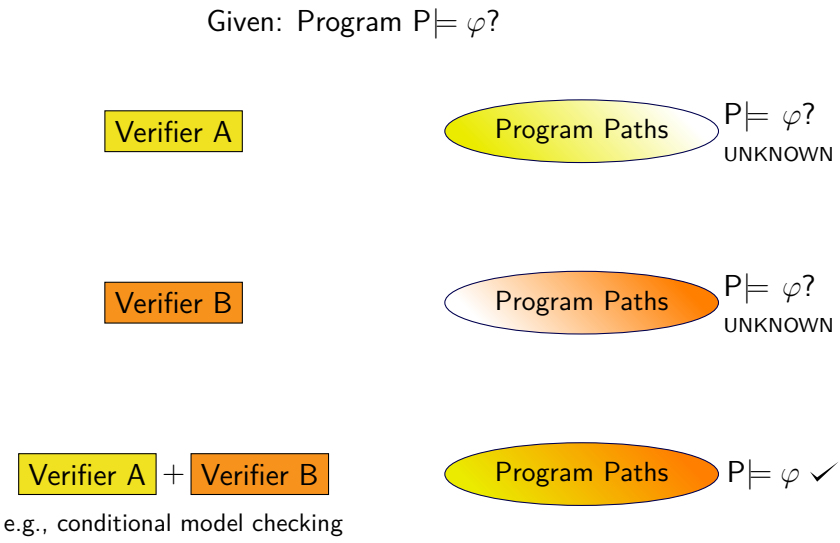
Results (#Tasks)	UAutomizer	2Ls	UAutomizer-R	CPAchecker-R
Correct 377	312	259	**333**	121
Proofs 264	250	189	**264**	55
Alarms 69	62	**70**	69	66

(A9) Facing Hard Verification Tasks

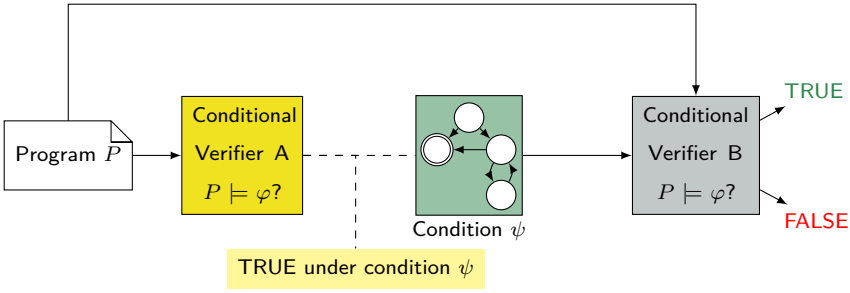
Given: Program P$\models \varphi$?



(A9) Facing Hard Verification Tasks

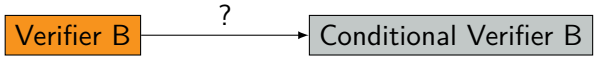


(A9) Conditional Model Checking



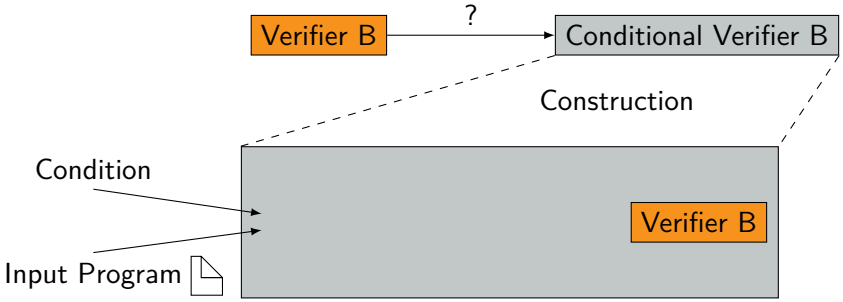
Proc. FSE 2012 [23]

(A10) Reducer-Based Construction



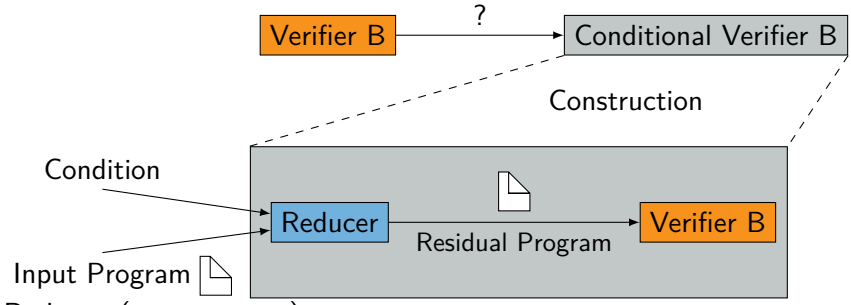
Proc. ICSE 2018 [26]

(A10) Reducer-Based Construction



Proc. ICSE 2018 [26]

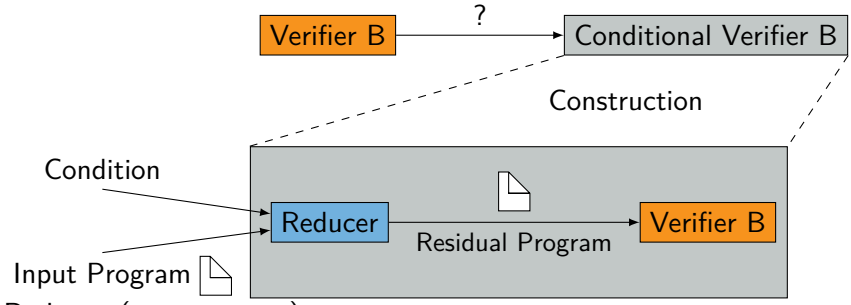
(A10) Reducer-Based Construction



- Builds standard input (C program)
- Representing a subset of paths
- Contains at least all non-verified paths

Proc. ICSE 2018 [26]

(A10) Reducer-Based Construction



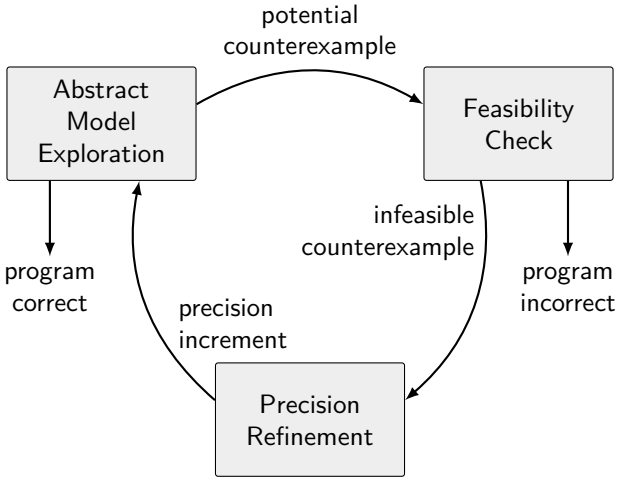
- Builds standard input (C program)
- Representing a subset of paths
- Contains at least all non-verified paths

\+ Verifier-unspecific approach

\+ Many conditional verifiers possible

Proc. ICSE 2018 [26]

(A11) CEGAR

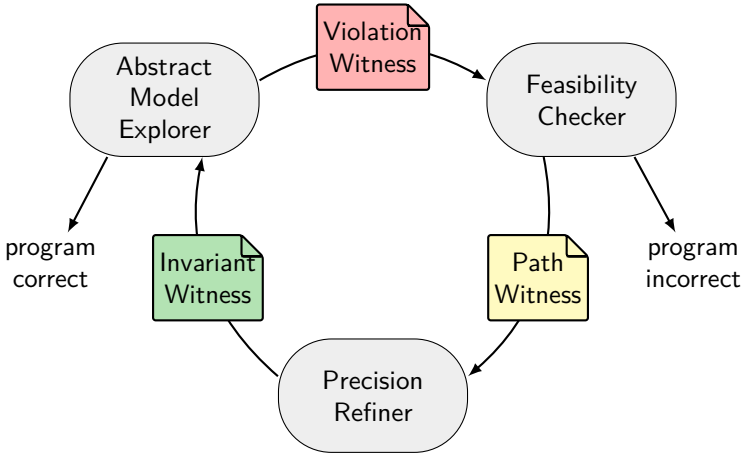

potential
counterexample
Abstract
Model
Exploration
Feasibility
Check
infeasible
counterexample
program
correct
program
incorrect
precision
increment
Precision
Refinement

(A11) Modularization of CEGAR

- CEGARdefines I/O interfaces
- But instances not exchangeable
- Aim: generalize CEGAR, allow exchange of components

$\Rightarrow$ Modular reformulation

(A11) Workflow of Modular CEGAR



Proc. ICSE 2022 [22]

(A12) Interactive and Automatic Methods

- How to achieve cooperation between automatic and interactive verifiers?
- Idea: Try to use existing interfaces for information exchange
- [37, Proc. SEFM '22]

```
//@ensures \return==0;
int main() {
  unsigned int x = 0;
  unsigned int y = 0;
  //@loop invariant x==y;
  while (nondet_int()) {
    x++;
    //@assert x==y+1;
    y++;
  }
  assert(x==y);
  return 0;
}
```

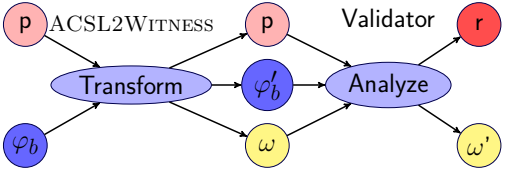
ACSL-annotated program, as used by FRAMA-C

```
...
<node id="q1">
<data key="invariant">( y == x )</data>
<data key="invariant.scope">main</data>
</node>
<edge source="q0" target="q1">
<data key="enterLoopHead">true</data>
<data key="startline">6</data>
<data key="endline">6</data>
<data key="startoffset">157</data>
<data key="endoffset">165</data>
</edge>
...
```

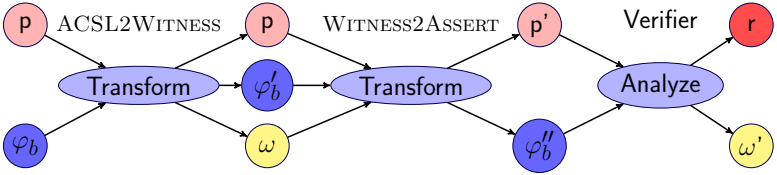
GraphML-based witness automaton generated by automatic verifiers

(A12) From Components: Construct Interactive Verifiers

- Turn a witness validator into an interactive verifier:



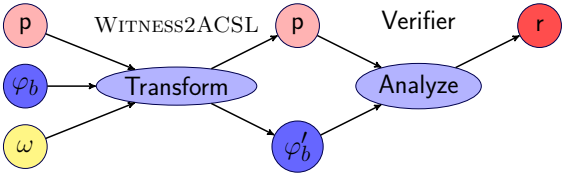
- Turn an automatic verifier into an interactive verifier:



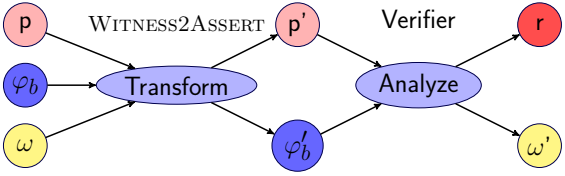
- Annotating in ACSL is more human-readable than witness automata
- Works for a wide range of automatic verifiers/validators

(A12) Component Framework: Constructing Validators

- Turn an interactive verifier (FRAMA-C) into a validator:

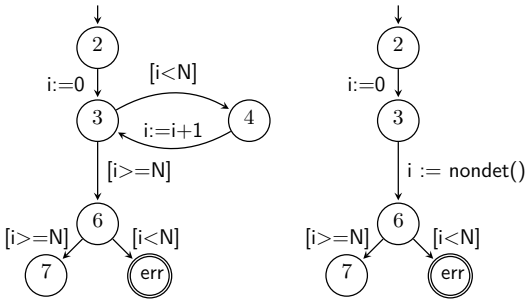


- Turn an automatic verifier into a validator [35, CAV '20]:



(A13) Loop Abstraction

```
1  void main() {
2    int i = 0;
3    while (i<N) {
4      i=i+1;
5    }
6    assert (i>=N);
7  }
```



- Instead of a precise acceleration, we can also apply an overapproximating *abstraction*
- Here we just havoc all variables that are modified in the loop, but more elaborate abstraction strategies exist

(A13) Example: Havoc Abstraction

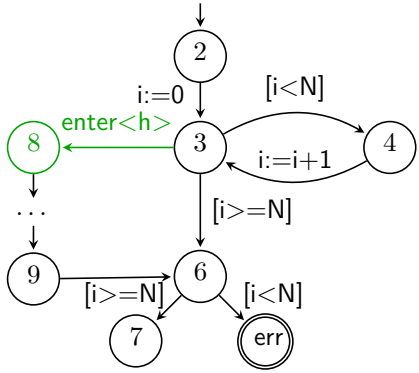
```
1  void main() {
2    int i = 0;
3    while (i<N) {
4      i=i+1;
5    }
6    assert (i>=N);
7  }
```

```
1  void main() {
2    int i = 0;
3    if (i<N) {
4      i = nondet();
5      assume(!(i<N));
6    }
7    assert (i>=N);
8  }
```

- Havoc Abstraction: if loop is entered, havoc all input variables of the loop and perform one loop iteration, then assume the loop is left
- Only sound if the loop body does not contain assertions
- Overapproximation, but sometimes enough (as in this example)

(A13) Configurable Solution a la CPAchecker

- Use the CFA as interface
- Add our loop abstractions next to the original loop
- Mark the entry nodes of each added alternative with an identifier for the applied strategy: $\sigma : L \to S$
- In the example:
  $S = \{b, h\}$
  $\sigma(8) = h$
  $\sigma(l) = b$ for all l except 8
- Select allowed strategies during state-space exploration using σ
- [32, Proc. SEFM '22]



(A13) Accessibility of Loop Abstractions via Patches

- We provide loop abstractions as patches
- We also output a the abstracted version of the program in case we found a proof
- Can be used independently by other tools
- Does this work in practice?
  $\Rightarrow$ Experiments

```
--- havoc.c
+++ havoc.c
-14,13 +14,16
    return ;
 }

 int main(void) {
   unsigned int x = 1000000;
- while (x > 0) {
- x -= 4;
+ // START HAVOCSTRATEGY
+ if (x > 0) {
+ x = __VERIFIER_nondet_uint();
   }
+ if (x > 0) abort();
+ // END HAVOCSTRATEGY
   __VERIFIER_assert(!(x % 4));
```

Why Transformation?

- Join forces
- Re-use verifier components off-the-shelf
- Divide and conquer
- Robust components because more widely used and tested
- Community involvement
- Have a tool chain and replace components for better ones
- Transformation tools as separate off-the-shelf components

Part 2: Verification Tools as Exchangable Components

Vision:

- All tools for formal methods work together to solve hard verification problems and make our world safer and more secure.
- Model checkers and theorem provers can be integrated into the software-development process as seamless as unit testing today.
- Model checkers, theorem provers, SMT solvers, and testers use common interfaces for interaction and composition.

Some Steps Towards the Vision

- **Find**: Which tools for software verification exist?
- ... for test-case generation?
- ... for SMT solving?
- ... for hardware verification?
- **Reuse**: How to get executables?
- Where to find documentation?
- Am I allowed to use it?
- How to use them?
- **Conserve**: Which operating system, libraries, environment?

Requirements for Solution

- Support documentation and reuse
- Easy to query and generate knowledge base
- Long-term availability/executability of tools
- Must come with tool support
- Approach must be compatible with competitions

Solution [12]

One central repository:
https://gitlab.com/sosy-lab/benchmarking/fm-tools which gives information about:

- Location of the tool (via DOI, just like other literature)
- License
- Contact (via ORCID)
- Project web site
- Options
- Requirements (certain Docker container / VM)
- Limits

Maintained by formal-methods community

Example: Entry for LTSmin [44]

```yaml
id: ltsmin
name: LTSmin
description: |
  LTSmin is a language-independent model-checking ...
input_languages:
  - B
  - DVE
  - ETF
  - PNML
  - Promela
  - ...
project_url: https://ltsmin.utwente.nl/
repository_url: https://github.com/utwente-fmt/ltsmin
spdx_license_identifier: BSD-3-Clause
benchexec_toolinfo_module:
   "https://www.cip.ifi.lmu.de/~wachowitz/ltsmin.py"
fmtools_format_version: "2.0"
fmtools_entry_maintainers:
  - ricffb
```

Example: LTSmin's Contacts

```yaml
maintainers:
  - orcid: 0000-0002-2433-4174
    name: Alfons Laarman
    institution: Leiden Institute for Advanced Computer Science
    country: Netherlands
    url: https://alfons.laarman.com/
```

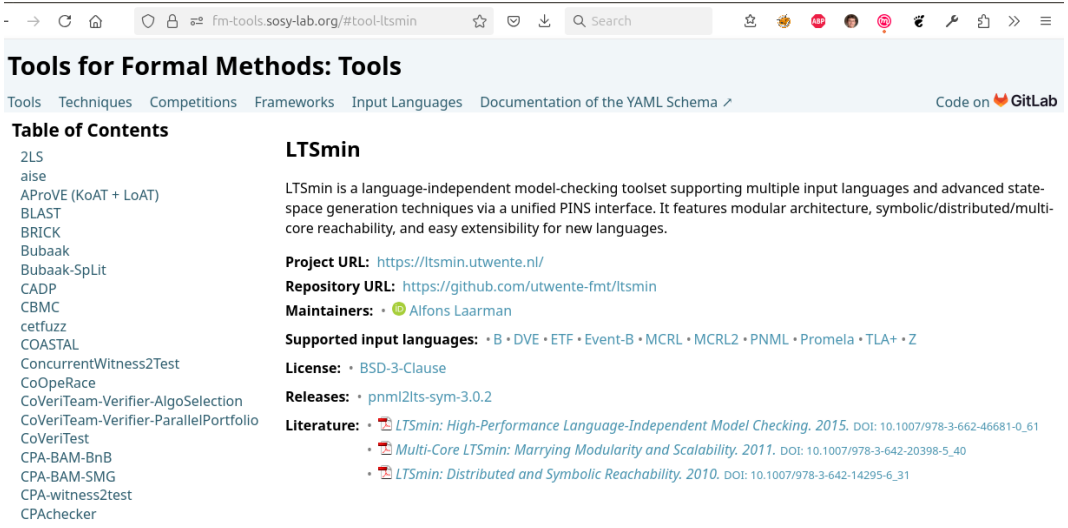
Example: LTSmin's Versions

```
versions:
  - version: "pnml2lts-sym-3.0.2"
    url:
       "https://github.com/utwente-fmt/ltsmin/releases/download/v3.0.2/ltsmin-v3.0.2-l
    benchexec_toolinfo_options: ["pnml2lts-sym"]
    required_ubuntu_packages: []
    base_container_image: ["ubuntu:24.04"]
```

Example: LTSmin's Documentation

```
literature:
  - doi: 10.1007/978-3-662-46681-0_61
    title: "LTSmin: High-Performance Language-Independent Model
       Checking"
    year: 2015
  - doi: 10.1007/978-3-642-20398-5_40
    title: "Multi-Core LTSmin: Marrying Modularity and
       Scalability"
    year: 2011
  - doi: 10.1007/978-3-642-14295-6_31
    title: "LTSmin: Distributed and Symbolic Reachability"
    year: 2010
```

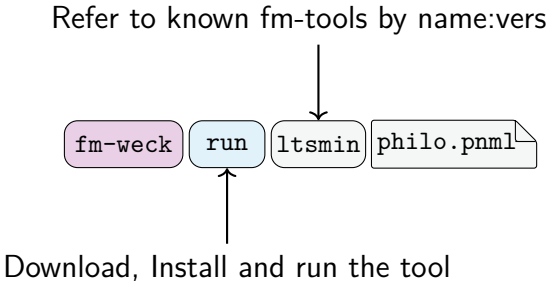
Example: LTSmin's Web-Page Entry



FM-Tools is FAIR

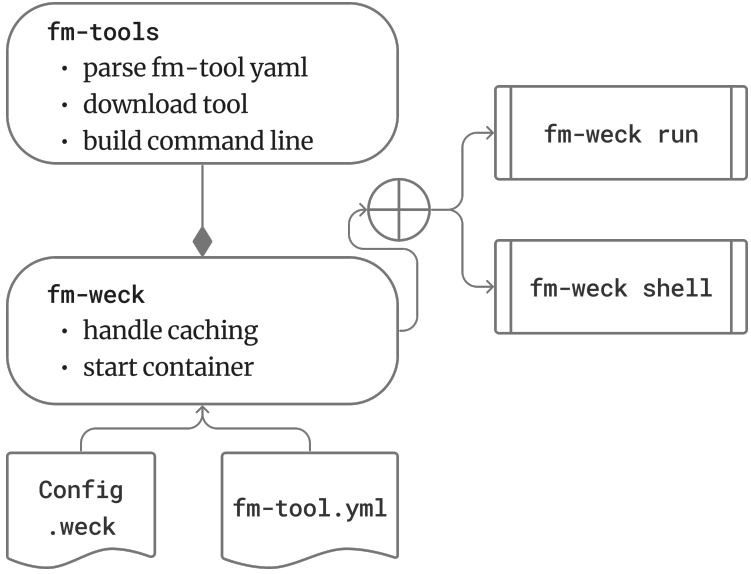
- **F**indable:
  overview is available on internet,
  generated knowledge base
- **A**ccessible:
  data retrievable via Git, format is YAML
- **I**nteroperable:
  Format is defined in schema,
  archives identified by DOIs, researchers by ORCIDs
- **R**eusable:
  Data are CC-BY, each tool comes with a license,
  format of tool archive standardized

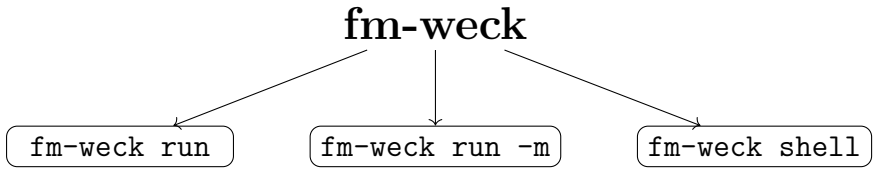
FM-Weck: Run Tools in Conserved Environment [39, Proc. FM 2024]



- No knowledge of the tools CLI needed
- Tool runs in a container (no dependencies on host system)

FM-Weck: Architecture





- Download and execute tool in container
- No knowledge of tool needed

- Download and execute tool in container
- Expert knowledge about tool required

- Spin up interactive shell in tool environment

Conclusion FM-Tools and FM-Weck

FM-Tools collects and stores essential information to:

- Generate a knowledge base about formal-methods tools [12]
  https://fm-tools.sosy-lab.org
- Conserve tool versions and their required environment
  (with help by Zenodo and Podman/Docker)
- Run a tool in conserved environment via FM-Weck [39]
- Please add your tool

https://fm-tools.sosy-lab.org

Conclusion

- Many verification tools and techniques
- External combinations are important
- Interfaces (artifacts, actors)
- Combinations and Cooperation
- Leverage Cooperation between Tools
- Conserve tools and make findable in FM-Tools

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