From Programs to Circuits:

Bridging Software and Hardware Model Checking with CPV and Pono

2025-12-22 Invited Talk @ NTU GIEE

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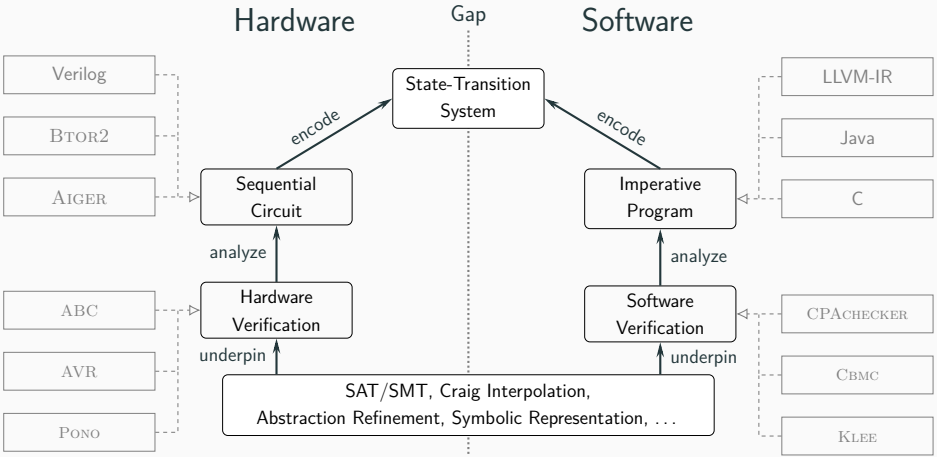
About Me

- Doctoral researcher at LMU Munich, Germany (since 2021)
  - Advised by Dirk Beyer and mentored by Nian-Ze Lee
- M.S. at NTU GIEE (2020)
  - Advised by Jie-Hong Roland Jiang
- B.S. at NTU EE (2018)
- Research interests: formal methods, hardware/software verification

Bridging Hardware & Software Verification

DFG project 536040111 – PIs: Dirk Beyer & Nian-Ze Lee



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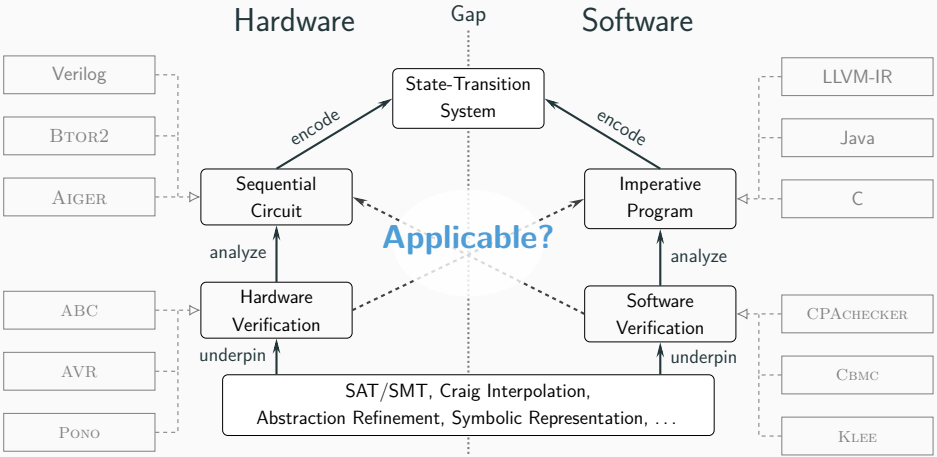
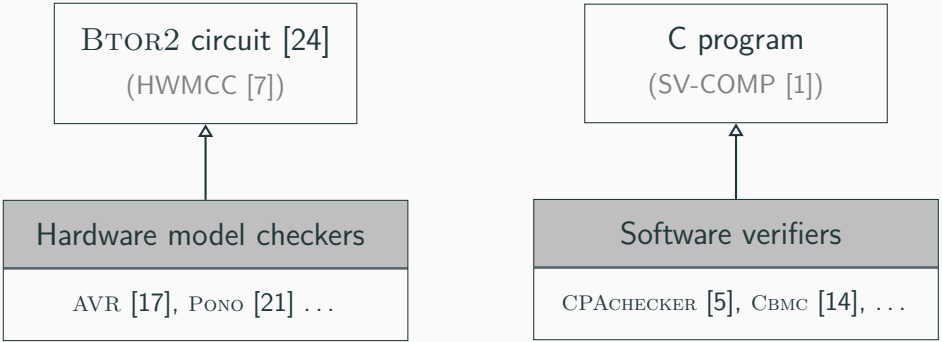


Verifying Software via Hardware Model Checking

BTOR2 circuit [24]
(HWMCC [7])

C program
(SV-COMP [1])

Verifying Software via Hardware Model Checking



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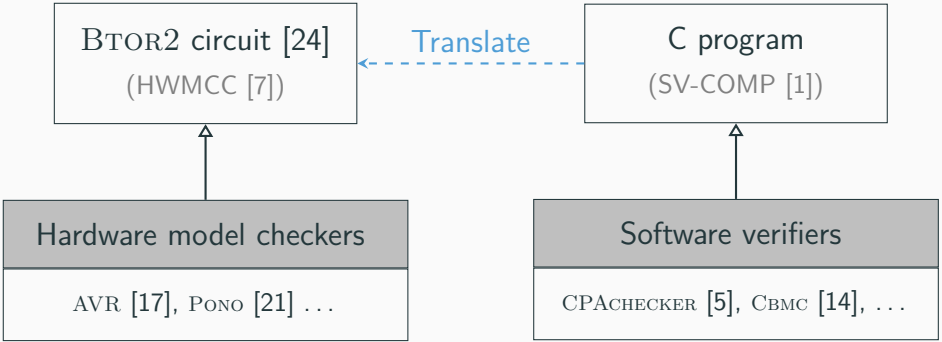

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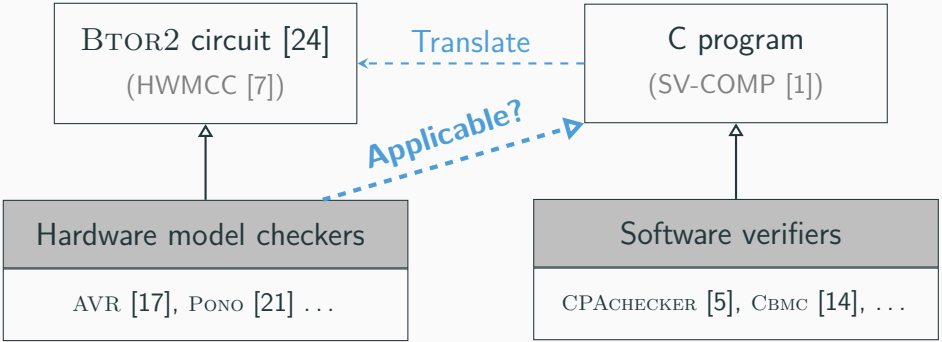

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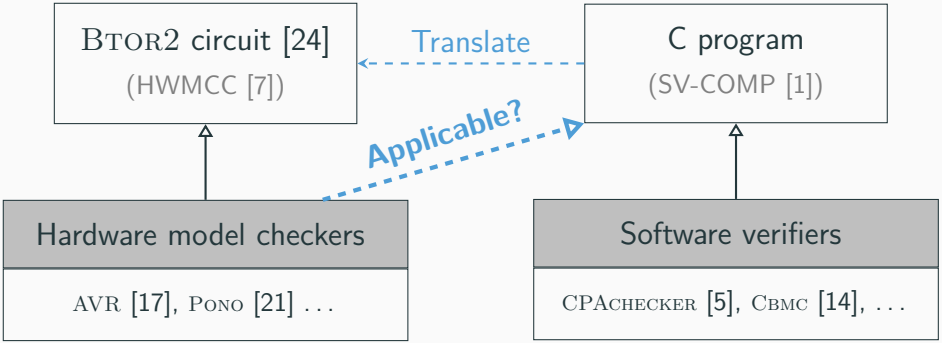


Could circuits serve as IR for program verification?

Outline

- CPV: A Circuit-Based Program Verifier

  https://gitlab.com/sosy-lab/software/cpv

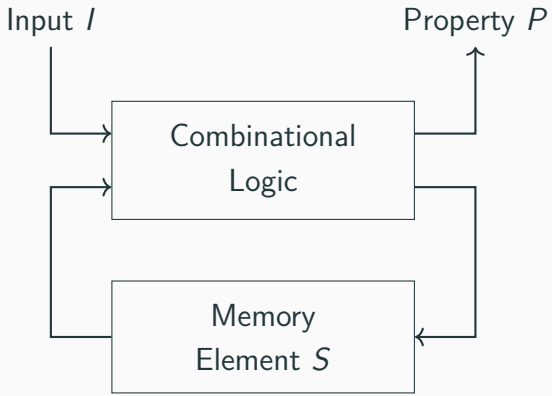
  - Translation pipeline: from C programs to sequential circuits
  - Verification backends and supported analyses
  - Experimental and competition results
- Pono: A Versatile SMT-Based Model Checker for Safety and Liveness

  https://github.com/stanford-centaur/pono

  - Architecture and solver-agnostic design
  - Recent developments in Pono 2.0
  - Comparison with other model checkers

Background

Hardware Model: Sequential Circuit



- State transition: $S' \leftarrow T_{func}(S, I)$
- Property: $P(S)$ or $P(S, I)$

Formats to Describe Circuits

Bit-level: Aiger

- Sorts: bool
- Ops: and, not

Word-level: Btor2

- Sorts: bitvec, array
- Ops: and, not, eq, add, mul, ite, read, write, ...

Example BTOR2 circuit:

```
1 sort bitvec 3
2 zero 1
3 state 1
4 init 1 3 2
5 input 1
6 add 1 3 5
7 one 1
8 sub 1 6 7
9 next 1 3 8
10 ones 1
11 sort bitvec 1
12 eq 11 3 10
13 bad 12
```

Hardware Model Checking

$$M \models \phi ?$$

Safety Property

Something bad never happens

$$\phi : \mathbf{G}\, P$$

Liveness Property

Something good eventually happens

$$\phi : \mathbf{F}\, P$$

Hardware Model Checking

$$M \vDash \phi?$$

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- Counterexample:

Liveness Property

Something good eventually happens

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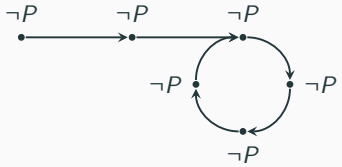


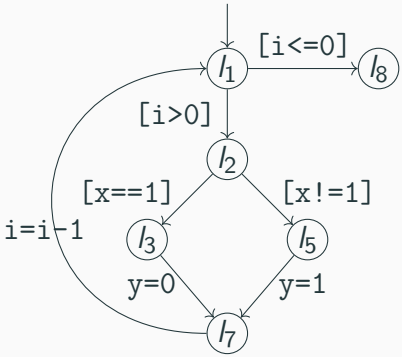
Model-Checking Algorithms

For checking safety properties:

- Bounded model checking (BMC) [9]
- k-induction (KI) [25]
- Interpolation-based model checking (IMC) [23]
- Property-directed reachability (IC3/PDR) [10, 15]
- Combined with CEGAR [13] using different abstraction techniques
  - Syntax-guided abstraction [16]
  - Predicate abstraction [19]

Software Model: Control-Flow Graph

```
1 while (i > 0) {
2   if (x == 1) {
3     y = 0;
4   } else {
5     y = 1;
6   }
7   i = i - 1;
8 }
```



Software Verification

$$M \models \phi?$$

Reachability Analysis (Safety)

Is an error location reachable?

$$\phi : \mathbf{G}\ \neg \mathit{error}$$

Termination Analysis (Liveness)

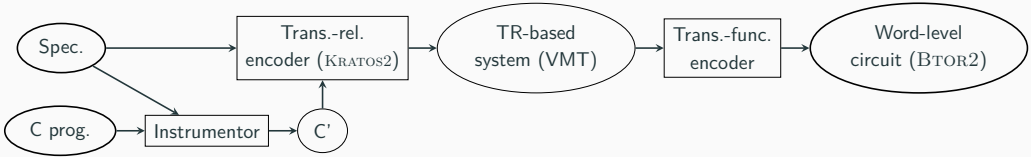
Can the program always terminate?

$$\phi : \mathbf{F}\ \mathit{end}$$

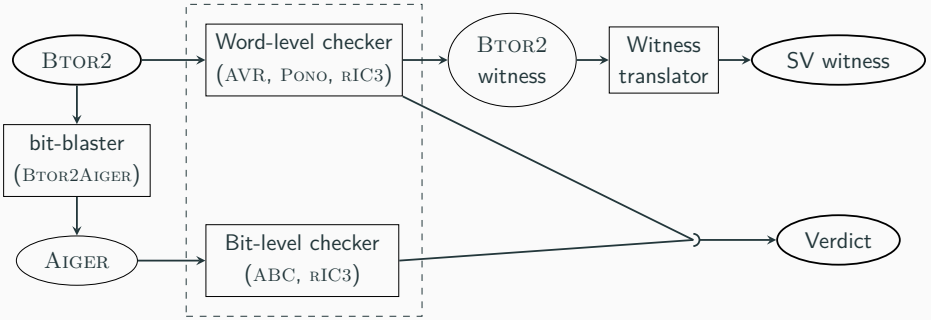
Circuit-Based Program Verification

Joint work with Dirk Beyer (LMU Munich),
Armin Biere (University of Freiburg), and
Nian-Ze Lee (National Taiwan University)

System Architecure: Frontend



System Architecure: Backend

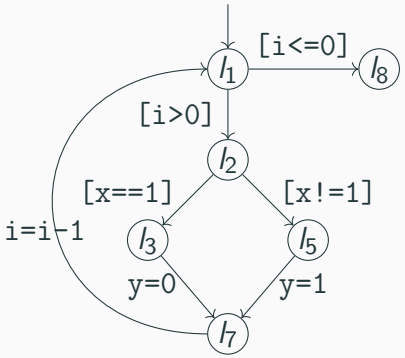


Managed by CoVeriTeam

Frontend: C Program → Transition Relation

Single-Block Encoding

C Program → Transition Relation

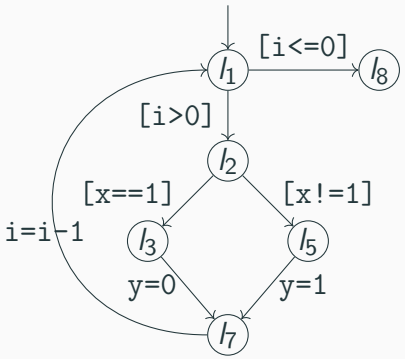


Each statement as a block:

$$TR = (pc = l_1 \wedge pc' = l_2 \wedge \mathbf{i} > \mathbf{0} \wedge i' = i \ldots)$$
$$\vee\, (pc = l_2 \wedge pc' = l_3 \wedge \mathbf{x} = \mathbf{1} \wedge i' = i \ldots)$$
$$\vee\, (pc = l_3 \wedge pc' = l_7 \wedge i' = i \wedge \mathbf{y}' = \mathbf{0} \ldots)$$
$$\vee \ldots$$

Large-Block Encoding

C Program → Transition Relation



Each loop-free section as a block:

$$TR = (pc = l_1 \wedge pc' = l_1 \wedge i > 0 \wedge i' = i - 1 \wedge y' = ite(x = 1, 0, 1) \ldots) \vee (pc = l_1 \wedge pc' = l_8 \wedge i \leq 0 \wedge i' = i \ldots) \vee \ldots$$

Encoding Details

C Program → Transition Relation

- KRATOS2 [18] is employed
- Large-block encoding [2] is used by default
- Function calls are inlined or treated as blocks
- C program uses `__VERIFIER_nondet_X()` to model nondeterministic values
  → Primary inputs in $TR(S, I, S')$

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- C program uses `__VERIFIER_nondet_X()` to model nondeterministic values
  → Primary inputs in $TR(S, I, S')$
- CPV vs. other software verifiers:
  Monolithic transition relation vs. ARG-based exploration [3]

Frontend: Transition Relation → Btor2 Circuit

Relational Encoding

Transition Relation → Btor2 Circuit

- Given $TR(S, I, S')$ and $P(S)$

Relational Encoding

Transition Relation → Btor2 Circuit

- Given $TR(S, I, S')$ and $P(S)$
- Auxiliary variables:
  - New state var *valid*
  - For each state var $s \in S$, introduce an input var s_{in}

Relational Encoding

Transition Relation → Btor2 Circuit

- Given $TR(S, I, S')$ and $P(S)$
- Auxiliary variables:
  - New state var *valid*
  - For each state var $s \in S$, introduce an input var s_{in}
- Transition *functions* and property in BTOR2:
  - $valid' \leftarrow valid \wedge TR(S, I, S_{in})$
  - $s' \leftarrow s_{in}$ for each $s \in S$
  - $P_{Btor2} : valid \Rightarrow P(S)$

Functional Encoding

Transition Relation → Btor2 Circuit

- Identify control and data flows in a block formula:

$$pc = l_1 \wedge pc' = l_1 \wedge i > 0 \wedge i' = i - 1 \wedge y' = ite(x = 1, 0, 1) \ldots$$

Functional Encoding

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$$pc = l_1 \wedge pc' = l_1 \wedge i > 0 \wedge i' = i - 1 \wedge y' = ite(x = 1, 0, 1) \ldots$$

- Derive next-state functions directly:

$$i' \leftarrow \begin{cases} i - 1 & , if\ pc = l_1 \wedge i > 0 \\ i & , if\ pc = l_1 \wedge i \leq 0 \\ \ldots & \end{cases}$$

Functional Encoding

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- TR is not right-total (e.g., $pc = l_{end}$ has no successor)
  → add an auxiliary sink state l_{sink}

Relational vs. Functional Encoding

Transition Relation → Btor2 Circuit

Relational

- More general (works for any transition relation)
- Usually result in smaller circuits

Functional

- Fewer input variables
- Allow optimization when circuits are unrolled [20]

Encoding Verification Property

Reachability Analysis (Safety)

Is an error location reachable?

```
int main() {  // l_init
  ...
  if (error_cond) {
    reach_error();  // l_err
  }
  ...
  return 0;
}
```

Termination Analysis (Liveness)

Can the program always terminate?

```
// instrumented by CPV
int main() {  // l_init
  // execute the original main
  original_main();
  // add termination marker
  reach_end();  // l_end
  return 0;
}
```

Encoding Verification Property

Reachability Analysis (Safety)

Is an error location reachable?

$$\phi : \mathbf{G}\,(pc \neq l_{err})$$

Termination Analysis (Liveness)

Can the program always terminate?

$$\phi : \mathbf{F}(pc = l_{end})$$

Encoding Verification Property

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- In BTOR2: `bad`
- Counterexample:

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Encoding Verification Property

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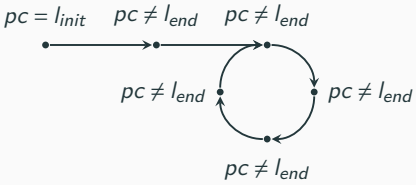
`justice` (+ `constraint`)



Backend: Model Checking

Integrated Hardware Model Checkers

	Tool	Input formats	Engines
Bit-level	ABC	AIGER	BMC, IMC, PDR
	rIC3	AIGER, BTOR2	BMC, KI, IC3
Word-level	AVR	BTOR2	BMC, KI, IC3sa
	PONO	BTOR2	BMC, IMC, KI, IC3sa, IC3ia

Implementation Details

- CoVeriTeam [4] is used to coordinate backend model checkers
  - Containerized execution with resource limits
  - Assemble command lines and extract tool outputs (logs and files)
  - Easy to combine multiple tools

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- CoVeriTeam [4] is used to coordinate backend model checkers
  - Containerized execution with resource limits
  - Assemble command lines and extract tool outputs (logs and files)
  - Easy to combine multiple tools
- Most tools do not support `justice` in Btor2
  → CPV does liveness-to-safety transformation

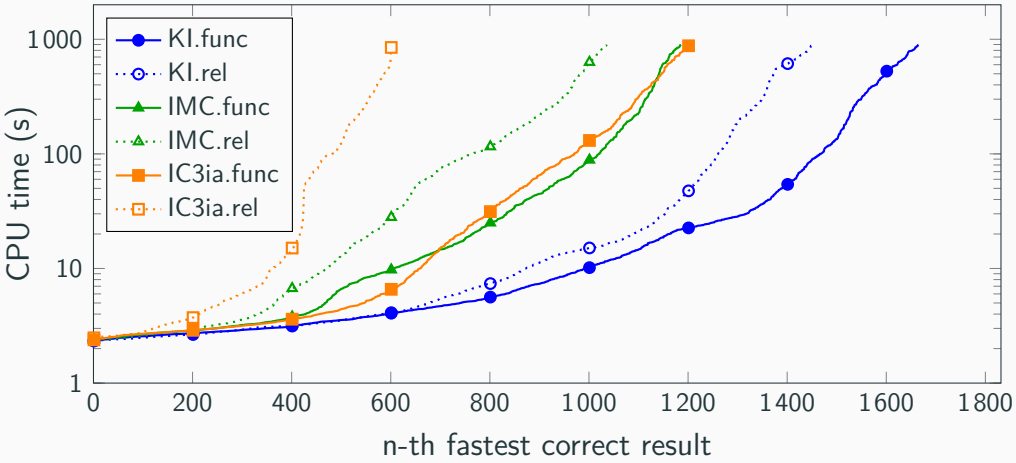
Current Limitations

- Lack support for many library functions (e.g., `<math.h>`)
- Limited support for recursion (*finite* unrolling)
- Does not handle concurrency
- Unsupported properties in SV-COMP:
  - Memory safety
  - Overflow detection

Experimental Evaluation

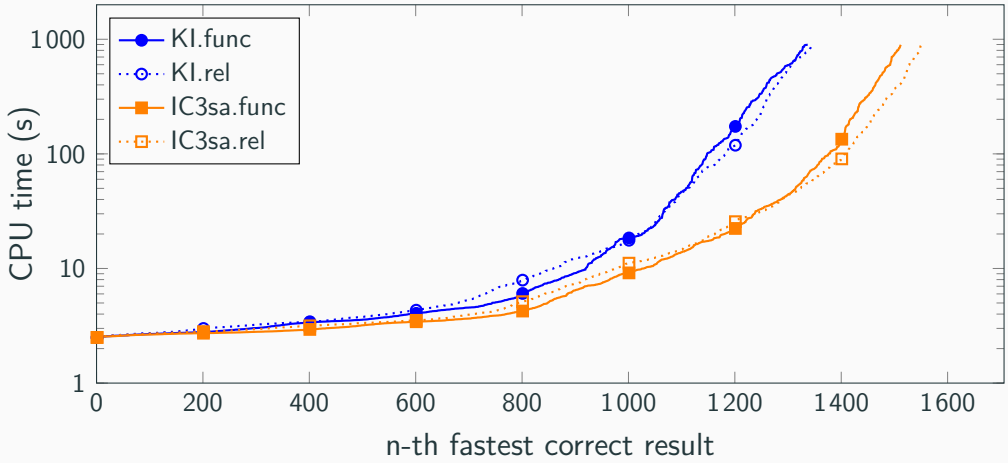
Experimental Results: Relational vs. Functional Encoding

Reachability analysis using Pono



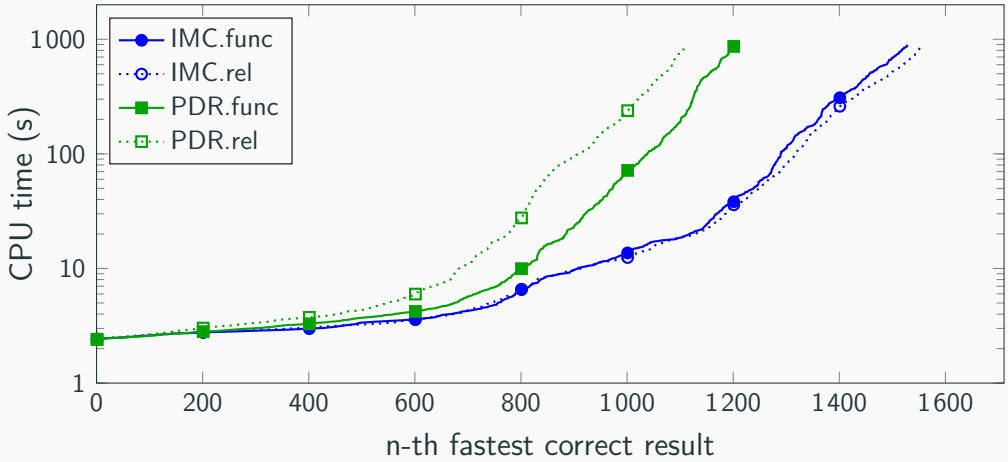
Experimental Results: Relational vs. Functional Encoding

Reachability analysis using AVR



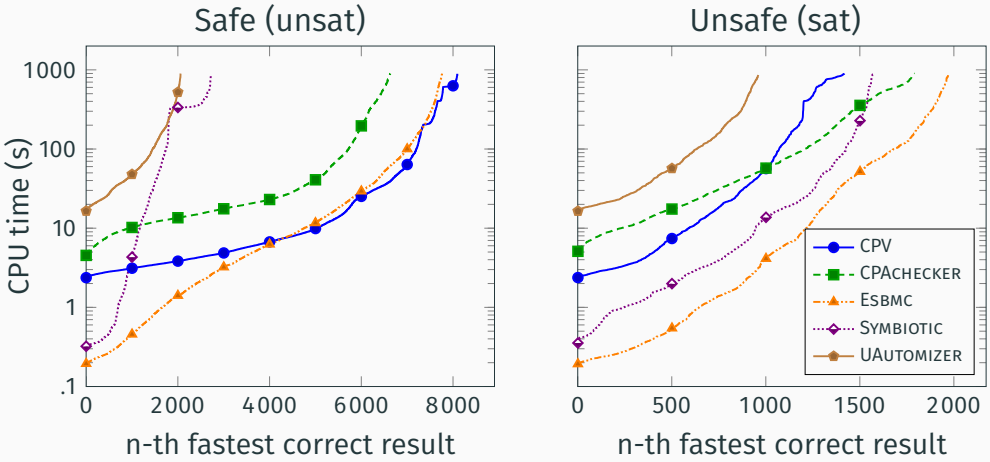
Experimental Results: Relational vs. Functional Encoding

Reachability analysis using ABC

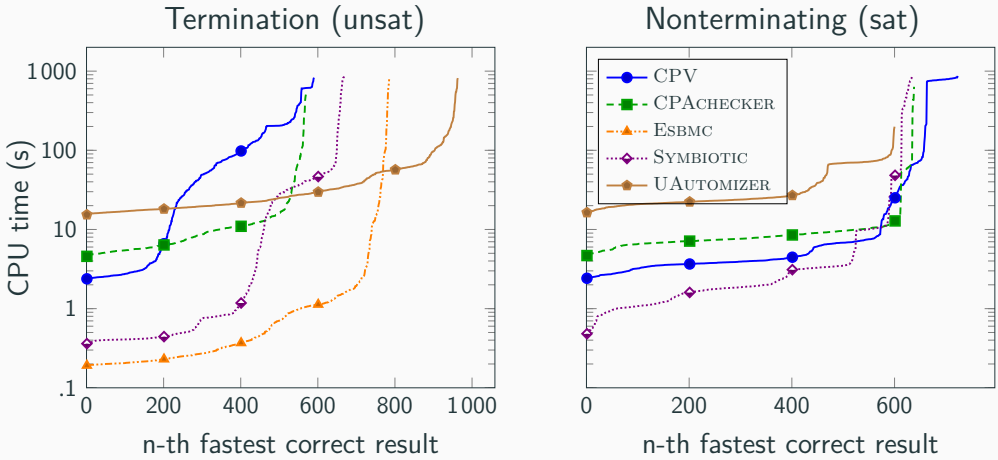


Preliminary Results in SV-COMP 2026: Reachability

Part of TACAS 2026 (April 11–16) @ Turin, Italy



Preliminary Results in SV-COMP 2026: Termination

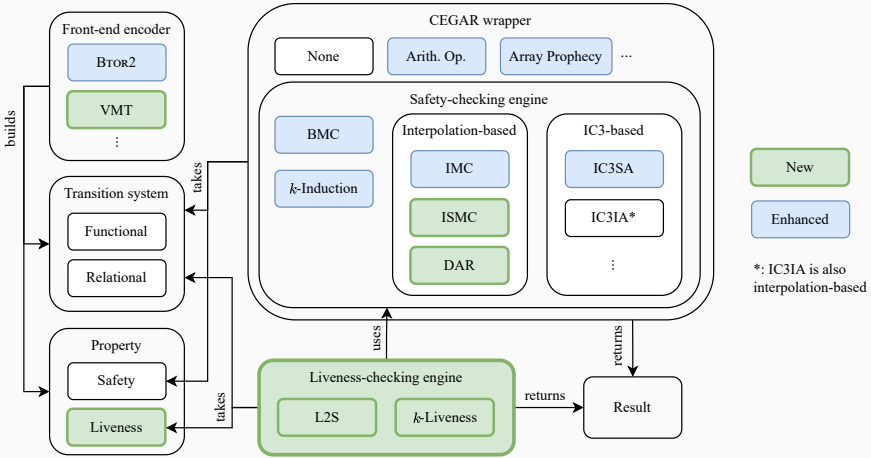


Pono:

A Versatile SMT-Based Model Checker

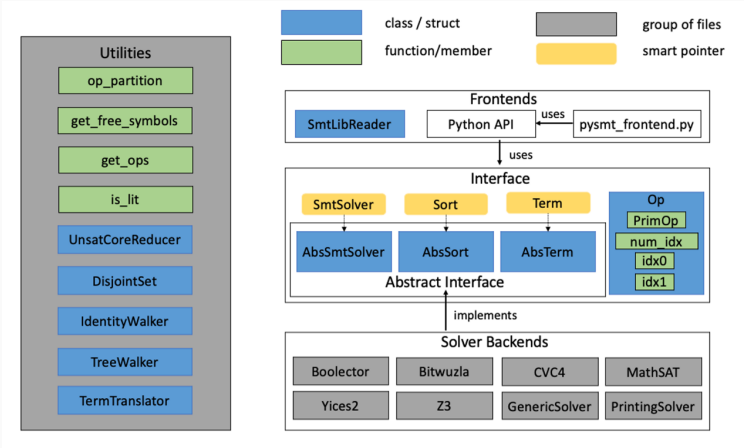
Joint work with Áron Ricardo Perez-Lopez[1], Florian Lonsing,
Samantha Archer[1], Ahmed Irfan[2], and Clark Barrett[1]
([1]Stanford University · [2]SRI International)

System Architecure



SMT Solver Integration

SmtSwtich: A Solver-Agnostic C++ API for SMT Solving

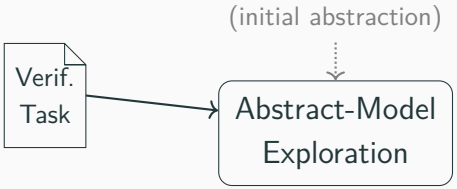


(Taken from [22])

New:

- Incremental interpolation
- BITWUZLA interpolation
- CVC5 integration

Counterexample-Guided Abstraction Refinement (CEGAR)



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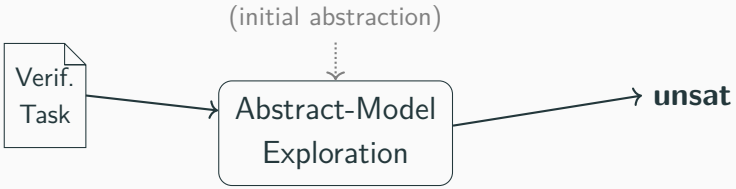

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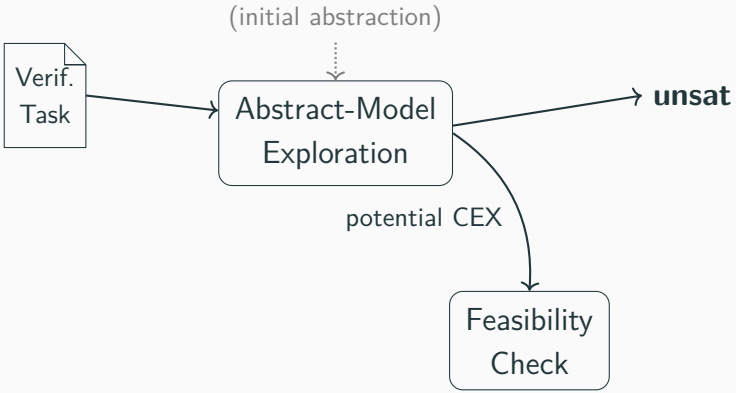

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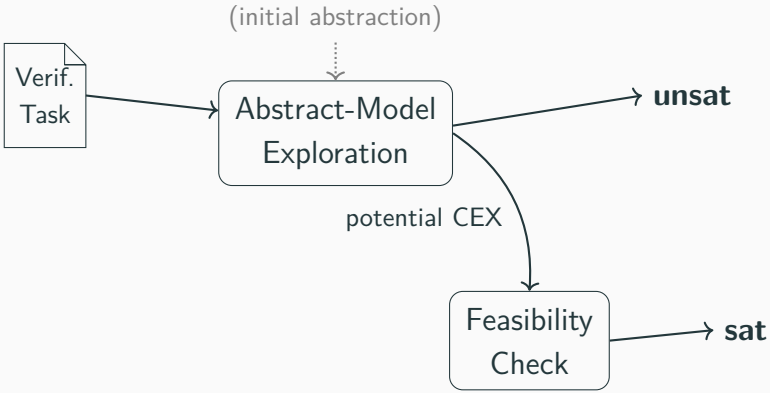

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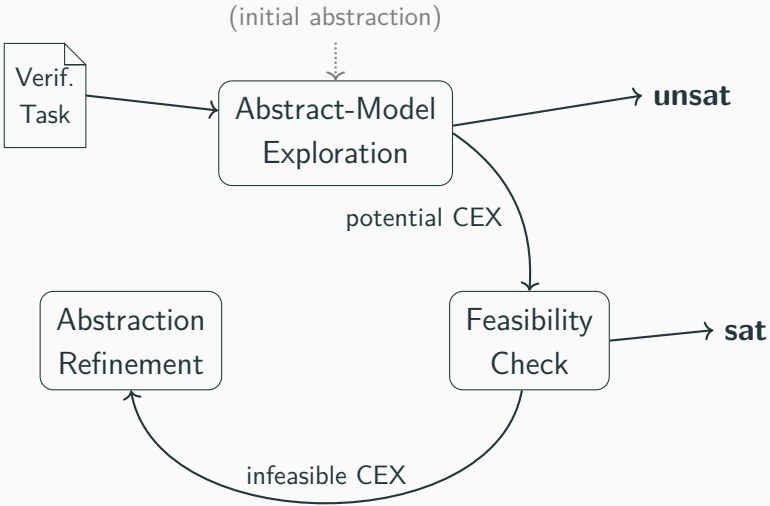

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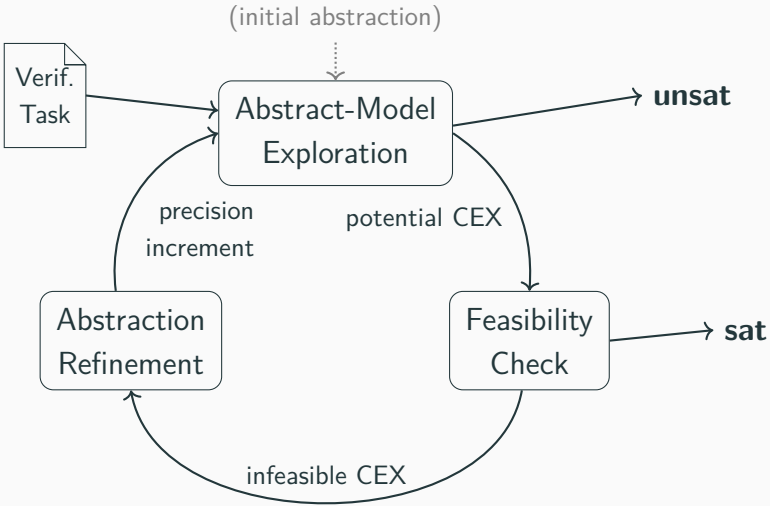

Arithmetic-Operation Abstraction

- SMT queries with complex arithmetic ops (e.g., $\div$, $\times$) are hard to solve
- Abstract these ops as uninterpreted functions (UFs) or free variables

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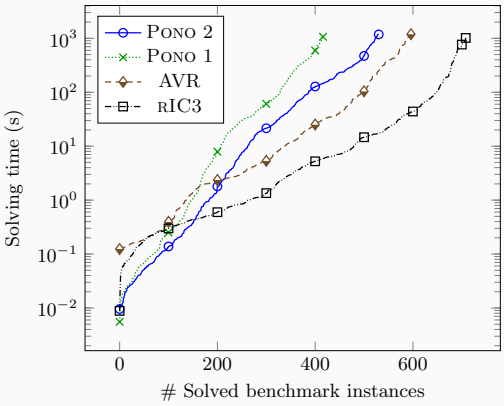
  - Check feasibility of the CEX with on concrete system
  - If unsat, identify ops to concretize from the unsat core
- Can be combined with any safety-checking engine in Pono

  (In version 1.0, only IC3IA and IC3SA)

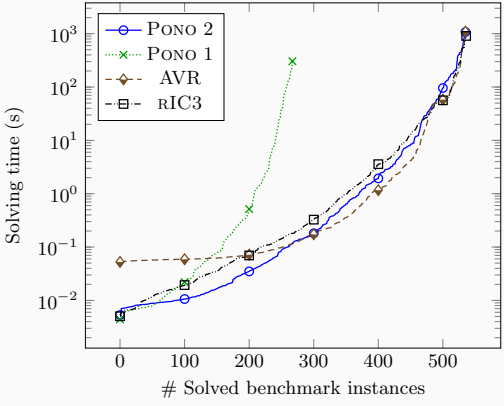
Liveness Checking

- Two approaches that reduce liveness to safety:
  - Liveness-to-Safety (L2S) [8]
  - *k*-liveness [12]
- Can be combined with any safety-checking engine in Pono
- Currently only works for finite-state systems (e.g., Btor2)
- If sat, Btor2 witness (lasso) can be exported

Evaluation: QF_BV Safety Checking

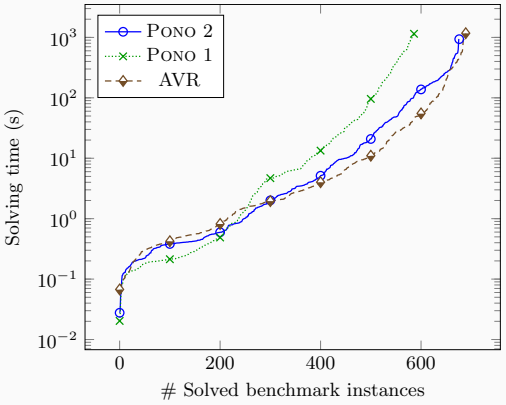


HWMCC tasks



SV-COMP Reachability tasks

Evaluation: QF_ABV Safety Checking



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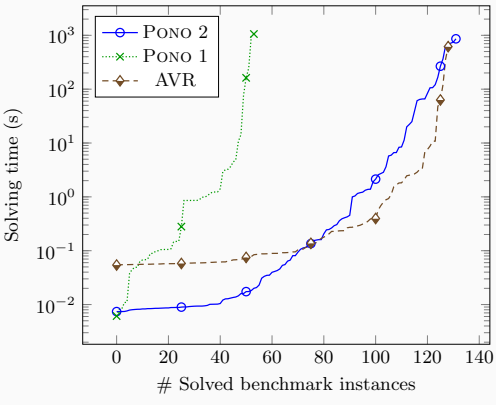
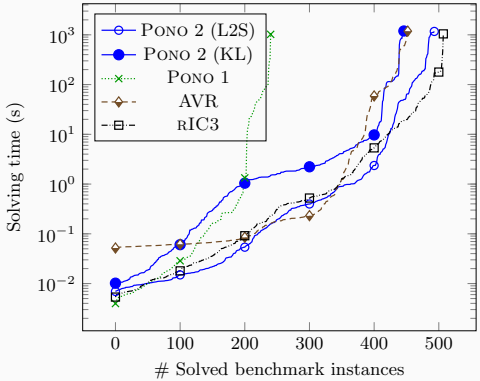
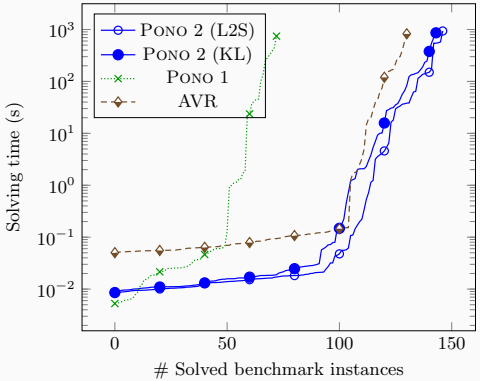


SV-COMP Reachability tasks

Evaluation: Liveness Checking



SV-COMP QF_BV Termination tasks



SV-COMP QF_ABV Termination tasks

(Pono 1, AVR, and rIC3 ran on pre-L2S-transformed tasks)

Conclusion

- CPV [11]
  - Encodes SV tasks as circuits
  - Leverages hardware model checkers as backend
- Pono [21]
  - Supports safety and liveness
  - Interfaces multiple SMT solvers
- Strong results in competitions
- Both projects are open-source

gitlab.com/
sosy-lab/software/cpv

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