From Programs to Circuits:

Bridging Software and Hardware Model Checking with CPV

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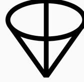
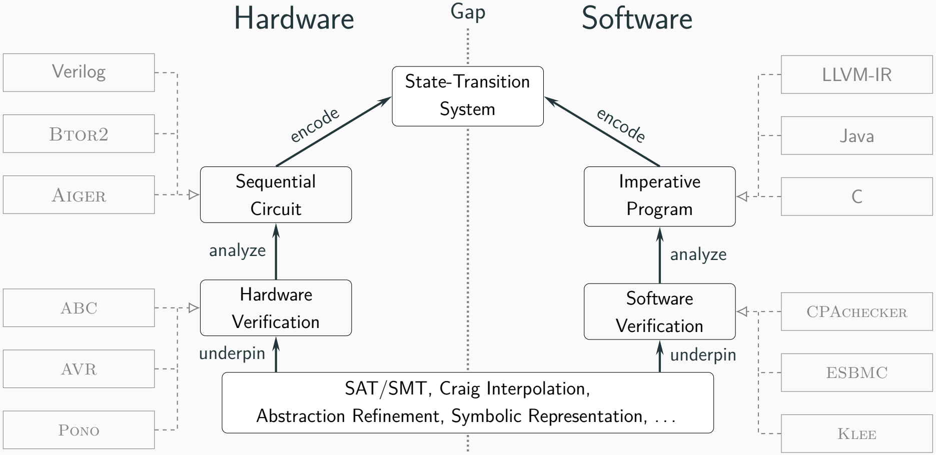


Bridging Hardware and Software Verification

DFG project 536040111 – PIs: Dirk Beyer and Nian-Ze Lee



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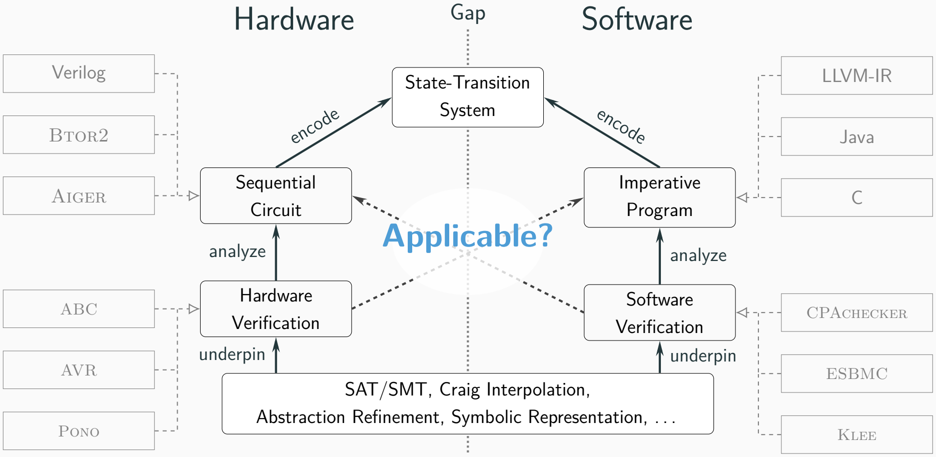


Verifying Software via Hardware Model Checking

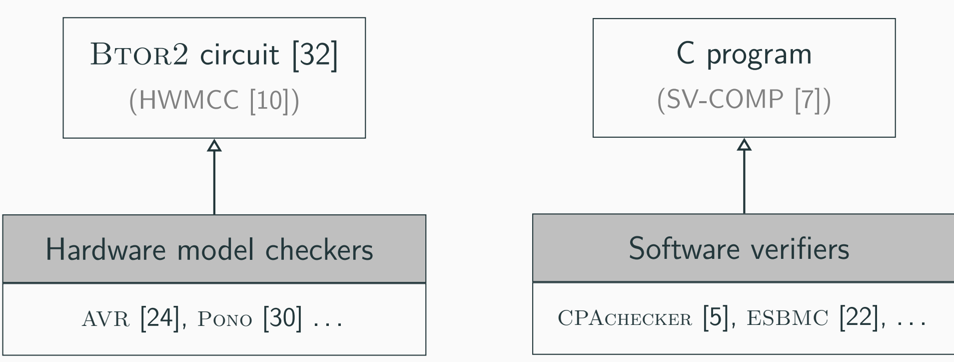
Btor2 circuit [32]

(HWMCC [10])

C program

(SV-COMP [7])

Verifying Software via Hardware Model Checking



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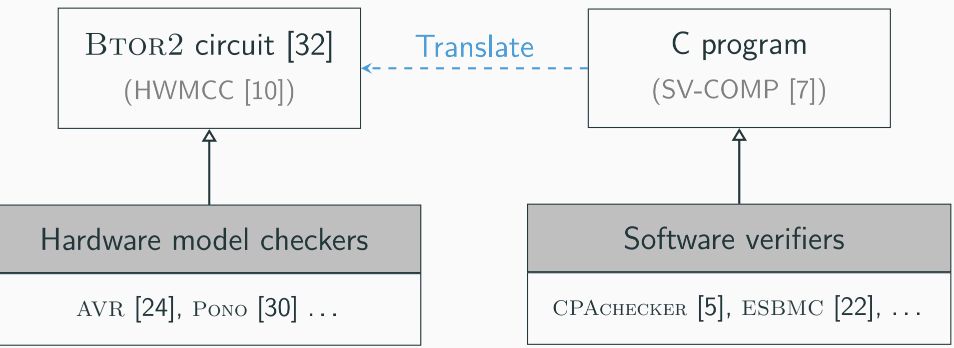

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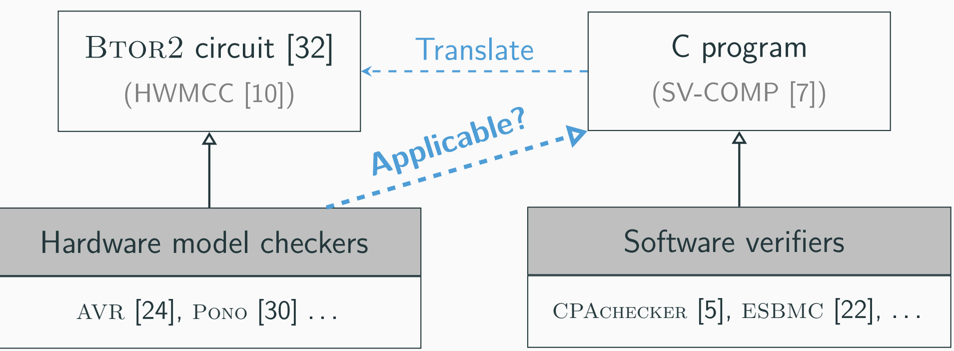

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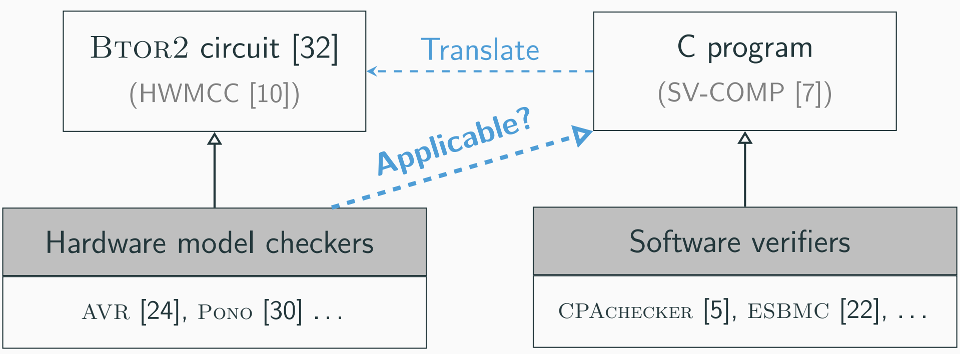


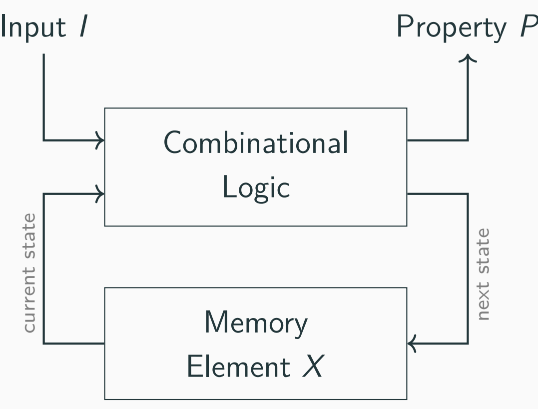
Could circuits serve as an IR for program verification?

Outline

- Background
- Verification pipeline of CPV
  - Encoding C verification tasks as sequential circuits
  - Hardware model checking
  - Witness translation
- Evaluation: Comparing to SOTA software verifiers

Background

Hardware Model: Sequential Circuit



- State transition: $X' \leftarrow T_{func}(X, I)$
- Property: $P(X)$ or $P(X, I)$

Hardware Model Checking

$$M \models \phi?$$

Safety Property

Something bad never happens

$$\phi : \mathbf{G}\, P$$

Liveness Property

Something good eventually happens

$$\phi : \mathbf{F}\, P$$

Hardware Model Checking

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- Counterexample:

$P \to P \to P \to P \to \neg P$

Liveness Property

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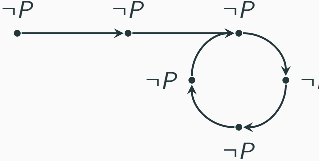


Software Model: Control-Flow Automaton

```
1  extern unsigned int nondet();
2  int main() {
3    unsigned int a = 1;
4    unsigned int b = nondet();
5    while (a <= b) {
6      a = nondet();
7      b = (b + 1) % 3;
8      if (a + b == 5) {
9        ERROR: return 1;
10     }
11   }
12   return 0;
13 }
```

Software Verification

$$M \models \phi?$$

Reachability Analysis (Safety)

Is an error location reachable?

$$\phi : \mathbf{G}\,\neg \mathit{error}$$

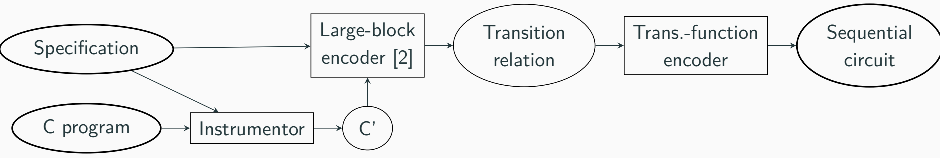
Termination Analysis (Liveness)

Can the program always terminate?

$$\phi : \mathbf{F}\,\mathit{end}$$

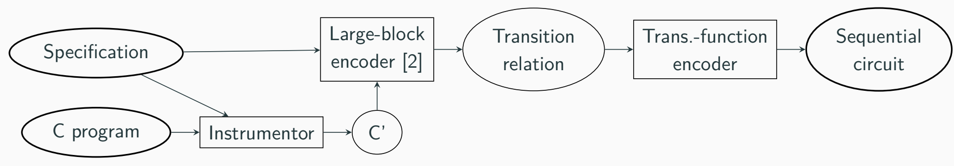
Verification Pipeline

Verification Pipeline of CPV



Frontend: Program instrumentation and encoding

Verification Pipeline of CPV



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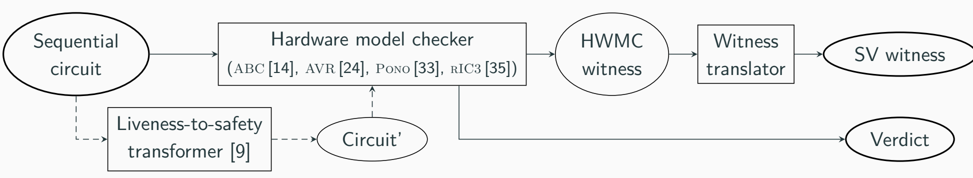
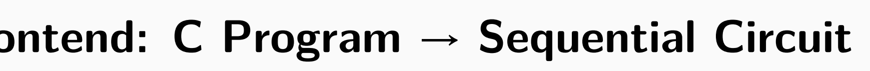


Backend: Model checking and witness translation

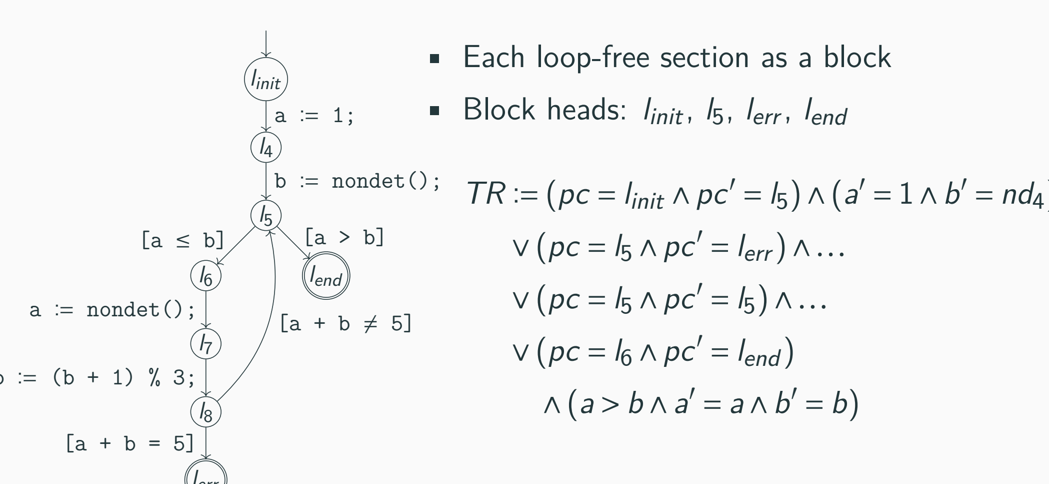
Design Principle

- Modular design with clear interfaces
- Exchange artifacts in standardized formats
  - Transition relation: VMT-LIB [17]
  - Sequential circuit: BTOR2 [32] (and AIGER [11])
  - HWMC witness: BTOR2
  - SV witness: GraphML (v1) and YAML (v2)


Frontend: C Program → Sequential Circuit

Large-Block Encoding

C Program → Transition Relation



LBE Details

C Program → Transition Relation

- Kratos2 [25] is employed (C → K2 IR → VMT-LIB)
- Function calls are inlined or treated as blocks
- `nondet()` calls are modeled by free input variables in TR

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- Function calls are inlined or treated as blocks
- `nondet()` calls are modeled by free input variables in TR
- CPV vs. other software verifiers:
  Monolithic transition relation vs. path-based exploration [3]

Functional Encoding

Transition Relation → Sequential Circuit

- Derive *explicit* next-state functions

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$$pc = l_6 \land pc' = l_{end} \land a > b \land a' = a \land b' = b \ldots$$

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- Next-state function for state variable a:

$$a' := \begin{cases} 1 & , if\ pc = l_{init} \\ nd_6 & , if\ pc = l_6 \land a \leq b \\ a & , if\ pc = l_6 \land a > b \\ * & , otherwise \end{cases}$$

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- TR is not right-total (e.g., $pc = l_{end}$ has no successor) → introduce l_{sink}

Encoding Verification Property

Reachability Analysis (Safety)

Is an error location reachable?

$$\phi : \mathbf{G}\,(pc \neq l_{err})$$

Termination Analysis (Liveness)

Can the program always terminate?

$$\phi : \mathbf{F}(pc = l_{end})$$

Encoding Verification Property

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- In BTOR2: `bad`
- Counterexample:

$pc = l_{init}$ → • → • → • → $pc = l_{err}$

Termination Analysis (Liveness)

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`justice` (+ `constraint`)

$pc = l_{init}$ → $pc \neq l_{end}$ → $pc \neq l_{end}$ → $pc \neq l_{end}$ → $pc \neq l_{end}$ → $pc \neq l_{end}$ → (back to the third state, forming a loop)

Backend: Model Checking

Model-Checking Algorithms

For checking safety properties:

- Bounded model checking (BMC) [12]
- k-induction (KI) [34]
- Interpolation-based model checking (IMC) [31]
- Property-directed reachability (IC3/PDR) [13, 21]
- Combined with CEGAR [19] using different abstraction techniques
  - Syntax-guided abstraction [23]
  - Predicate abstraction [27, 18]

Integrated Hardware Model Checkers

	Tool	Input formats	Engines
Bit-level (QF_BV)	ABC	Aiger	BMC, IMC, PDR
	rIC3	Aiger, Btor2	BMC, KI, IC3
Word-level (QF_ABV)	AVR	Btor2	BMC, KI, IC3sa
	Pono	Btor2	BMC, IMC, KI, IC3sa, IC3ia

Implementation Details

- Use CoVeriTeam [4] to coordinate backend model checkers
  - Containerized execution with resource limits
  - Assemble command lines and extract tool outputs (logs and witnesses)
  - Easy to combine multiple tools

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- Use CoVeriTeam [4] to coordinate backend model checkers
  - Containerized execution with resource limits
  - Assemble command lines and extract tool outputs (logs and witnesses)
  - Easy to combine multiple tools
- Most tools do not support `justice` in Btor2
  → CPV does liveness-to-safety transformation [9]

Witness Translation

- HWMC witness:

Time step	State			Input	
	pc	a	b	nd_4	nd_6
0	l_{init}	-	-	`UINT_MAX`	-
1	l_5	1	`UINT_MAX`	-	**5**
2	l_{err}	5	0	-	-

Witness Translation

- HWMC witness:

Time step	State			Input	
	pc	a	b	nd_4	nd_6
0	l_{init}	-	-	`UINT_MAX`	-
1	l_5	1	`UINT_MAX`	-	**5**
2	l_{err}	5	0	-	-

- SV witness (test case): Enter `main`
  → `nondet()` returns **`UINT_MAX`** at line 4
  → `nondet()` returns **5** at line 6
  → reach `ERROR`

Current Limitations of CPV

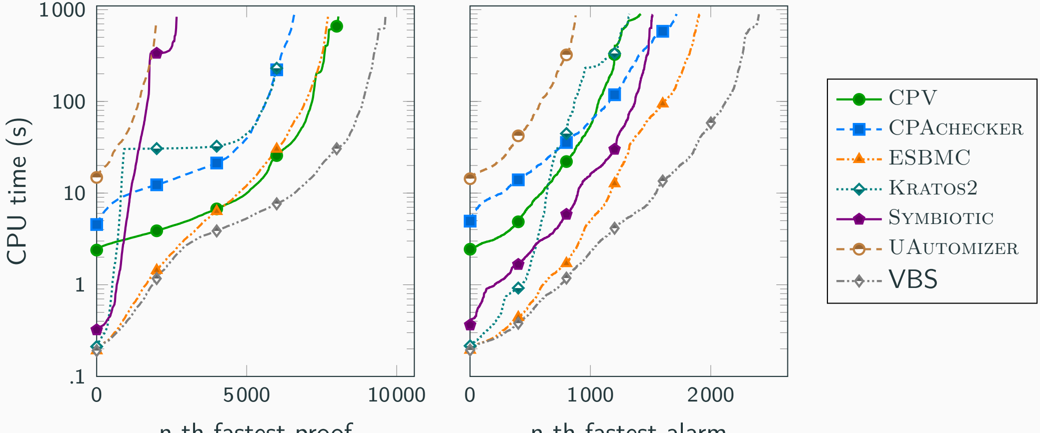
- Lack modeling for many library functions (e.g., `<math.h>`)
- Limited support for recursion (*finite* unrolling)
- Does not handle concurrency
- No support yet for correctness witness (invariant) translation
- Unsupported properties in SV-COMP:
  - Memory safety
  - Overflow detection

Experimental Evaluation

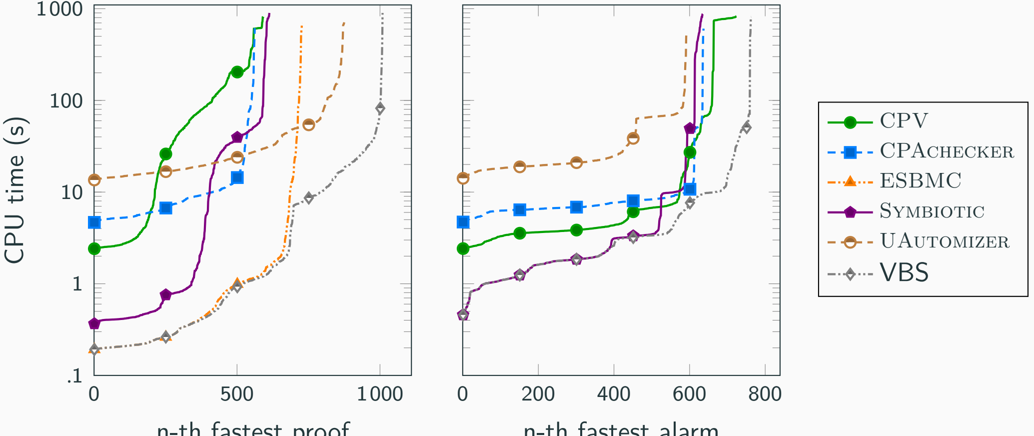
Experimental Setup

- Benchmark sets:
  ReachSafety and *Termination* tasks from SV-COMP 2026 without recursion
- Compared CPV 1.1 [16] against CPAchecker [8], ESBMC [29], Kratos2 [26], Symbiotic [1], and UAutomizer [20]
  (running in SV-COMP configurations)
- Resource limits for each run:
  15 min of CPU time, 15 GB of memory, and 2 CPU cores
- Reliable benchmarking by BenchExec [6]

Experimental Results: SV-COMP ReachSafety



Experimental Results: SV-COMP Termination



Experimental Results: Highlights

ReachSafety

1st:

- #Proofs overall
- Subcategories: *BitVectors*, *Hardware*

2nd:

- #Solved overall
- Subcategories: *Arrays*, *Hardness*, *ProductLines*, *XCSP*

Termination

1st:

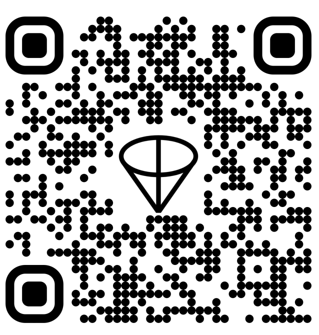
- #Alarms overall
- Subcategory: *Other*

2nd:

- #Solved overall
- Subcategory: *BitVectors*

Conclusion

- With CPV [15], we can
  - encode SV tasks as circuits
  - leverage powerful hardware model checkers as backend
- Strong performance in SV-COMP!
- Submitted translated BTOR2 circuits to HWMCC
- Next steps:
  - Correctness witness translation
  - Extend frontend support



gitlab.com/sosy-lab/software/cpv

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