CPV: A Circuit-Based Program Verifier

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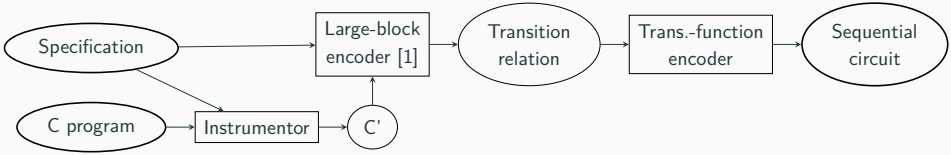
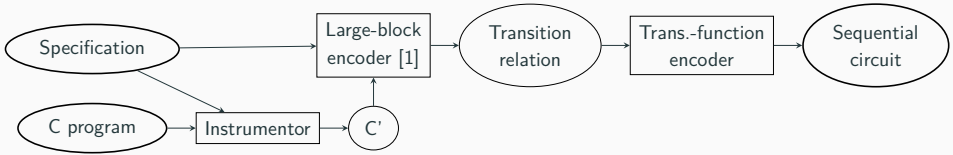
Verification Pipeline of CPV

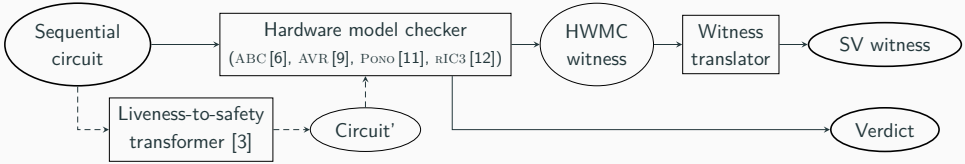


Frontend: Program instrumentation and encoding

Verification Pipeline of CPV



Frontend: Program instrumentation and encoding

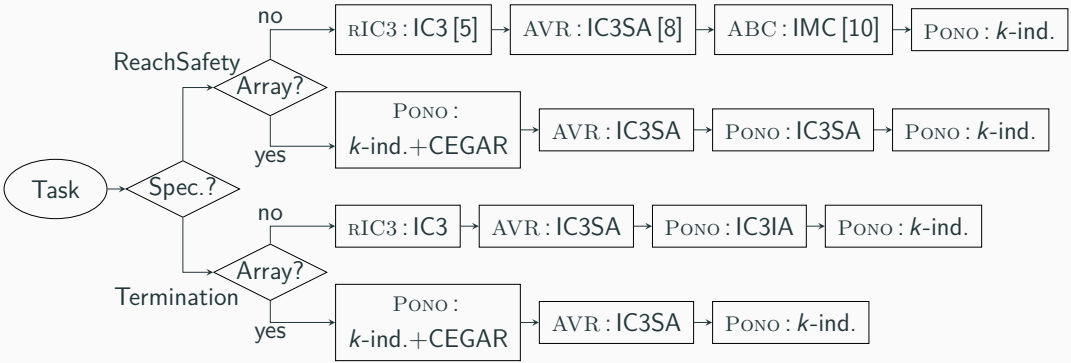


Backend: Model checking and witness translation

Enhancements for SV-COMP 2026

- Support Termination analysis (via liveness-to-safety reduction [3])
- Export violation witness v2
- Fix several issues in frontend task translator
- Integrate 2 new backend hardware model checkers: Pono [11] and rIC3 [12]
- Design a new strategy for SV-COMP

Strategy for SV-COMP 2026



CPV's Results at SV-COMP 2026: Highlights

C.ReachSafety

🥇 **1st:**

- Most #proofs overall (confirmed + unconfirmed)
- BitVectors, Hardware

🥈 **2nd:**

- 2nd most #solved overall (confirmed + unconfirmed)
- ECA, ProductLines, XCSP

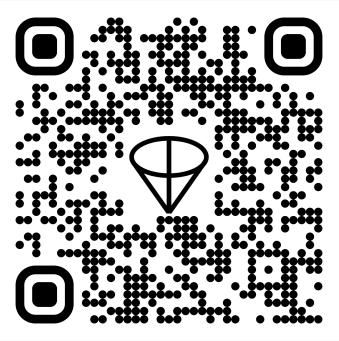
🥉 **3rd:** Arrays, Combinations, Hardness, Sequentialized

C.Termination

🥉 **3rd:** BitVectors

Conclusion

- With CPV [7], we
  - encode SV tasks as circuits
  - leverage powerful hardware model checkers as backend
- Strong performance in SV-COMP [2]
- Submitted translated BTOR2 circuits to HWMCC [4]
- Next steps:
  - Correctness witness translation
  - Extend frontend support



gitlab.com/
sosy-lab/software/cpv

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