A Case Study in Firmware Verification

Applying Formal Methods to Intel TDX Module

Dirk Beyer[1], Po-Chun Chien[1], Bo-Yuan Huang[2]
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SoSy-Lab Software Systems

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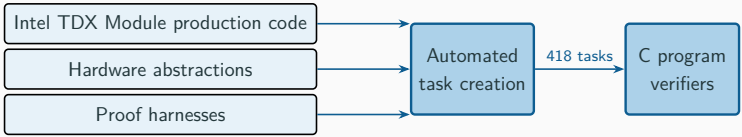
This Talk

Applying automatic verifiers for C programs to industry-scale firmware

Extend a code-level model-checking methodology [1] with **hardware abstractions**



Evaluating representative verifiers (e.g., CBMC, KLEE) covering diverse techniques

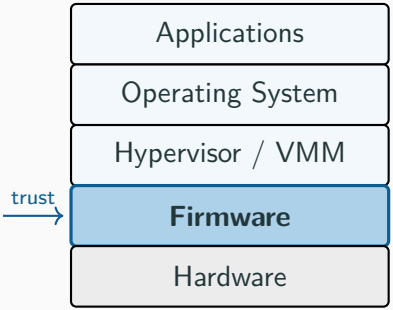
Only **59 %** tasks solved by *any* of the evaluated tools

Project webpage

INT31 blog post

Why Firmware Verification?

Firmware: Foundation of System Security



- Orchestrates **boot**, **hardware initialization**, and **security enforcement**
- Operates at **lowest, most privileged** layer

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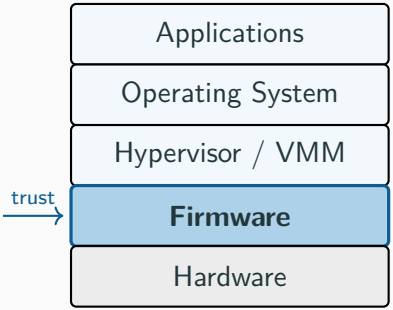

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The trustworthiness of all upper layers rests on firmware correctness.

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- **Manual code review** by security experts
- **Fuzzing** and handcrafted test suites

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Example: security reviews of **Intel TDX 1.5** by Google [2] and Microsoft [3]

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  - Published in February 2026, five Google researchers over six months

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Effective but **labor-intensive** and **hard to scale** – and the *negative space* (adversarial, unforeseen inputs) is hard to cover by testing.

Automatic Verification for C Programs

- Firmware: mostly written in **C** (plus assembly)
- Mature ecosystem of automatic verifiers and success stories

  CBMC, ESBMC, KLEE, CPACHECKER, MOPSA, UAUTOMIZER, ... (cf. SV-COMP [4])
- Yet scarce application to firmware

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Research question: How can automatic verifiers for C programs be applied to **efficiently** and **effectively** check specification conformance and detect vulnerabilities in firmware?

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  Behaviors depend on firmware and hardware states

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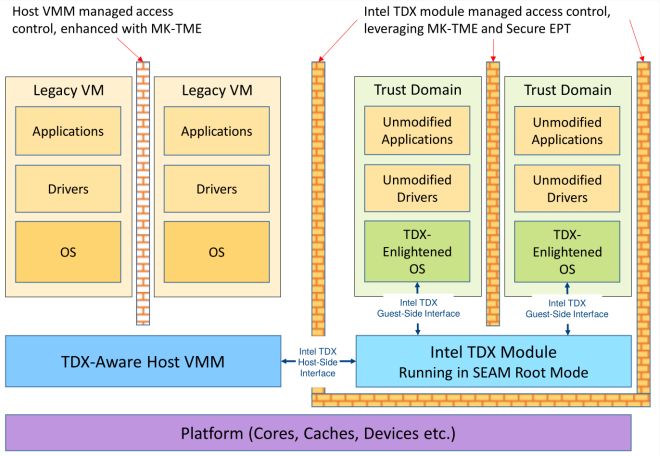
  → Symbolic initialization + constraining (for modular analysis)

Designing the Case Study

Intel TDX Module: Hardware-Enforced VM-Level Isolation



Source: Fig. 2.1 in Intel TDX Module v1.5 Base Architecture Spec. [5]

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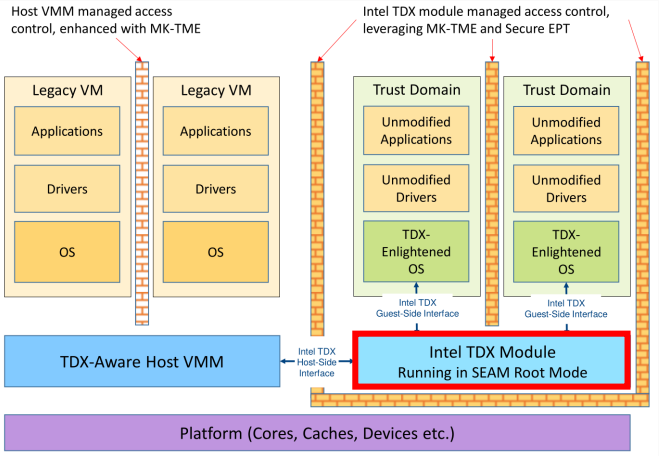

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- Host: VMM
- Guest: TD
- Communicate via ABI to protect “data in use”

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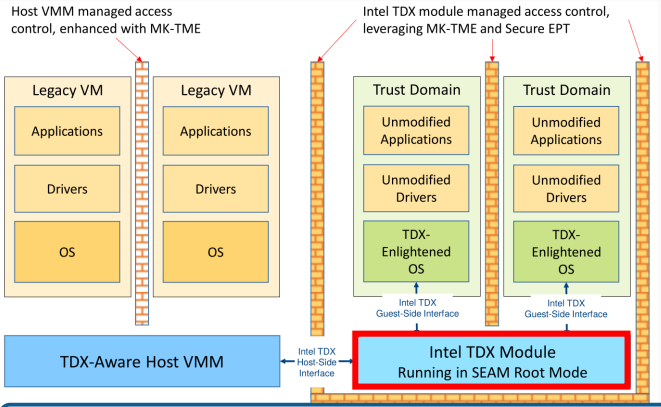

- Host: VMM
- Guest: TD
- Communicate via ABI to protect "data in use"

Goal: Verify the ABI of TDX Module (a prime attack surface), assuming VMM and TDs can call any interface function with arbitrary inputs.

Hardware Abstraction

Enable C verifiers to reason about firmware–hardware interactions

- **Standard x86 instructions** (e.g., `MOV`, `CMPXCHG`)
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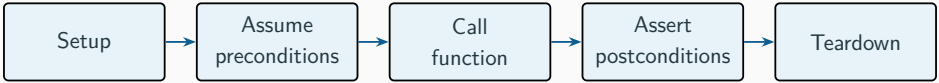
- **Memory-mapped regions** (e.g., SEAMLDR-initialized module state)
  → Replace with **mock variables**

```
tdx_module_local_t *get_local_data(void) {
#ifdef TDXFV_NO_ASM
  return &local_data_fv; // mock
#else
  uint64_t local_data_addr;
  _ASM_("movq %%gs:%c[local_data], %0\n\t"
        : "=r"(local_data_addr)
        : [local_data] "i"(offsetof(tdx_module_local_t, local_data_fast_ref_ptr)));
  return (tdx_module_local_t *)local_data_addr;
#endif
}
```

Proof-Harness Design

Five-step harness design for code-level model checking [1]



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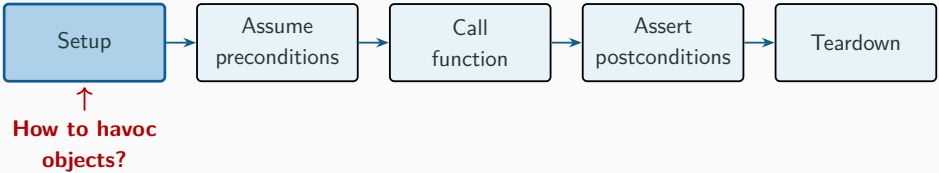

Havocking strategies for symbolic initialization:

- **Memory havocking**: byte by byte
- **Object havocking**: field by field
- **Tool-specific**: `__CPROVER_havoc_object`, `klee_make_symbolic`, ...

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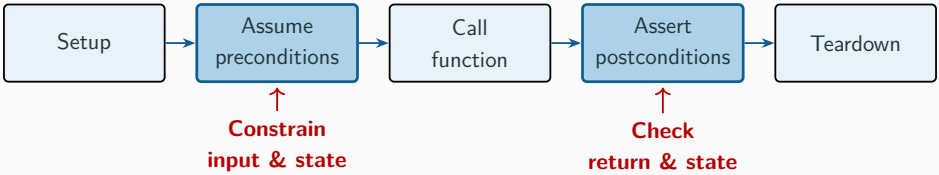

Verification properties (manually derived from TDX specification):

- **Functional correctness**: correct execution or error handling
- **State integrity**: registers not modified unexpectedly
- **Cover points**: inserted after precondition, function call, and teardown

Selection of Interface Functions

- Selection criteria:
  - At least one function from each functional class
  - At least one function permitted in each lifecycle stage
  - All functions that trigger lifecycle transitions

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- 16 of 77 host-side functions (`TDH.*`)
- 6 of 31 guest-side functions (`TDG.*`)

Study Results and Diagnosis

Evaluation Results

Evaluated verifiers:
CBMC [6], ESBMC [7], KLEE [8],
CPACHECKER [9], MOPSA [10], UAUTOMIZER [11]

Computing resources per task:

- 60 min CPU time
- 30 GB memory

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59 % of tasks encoded with tool-specific havocking primitives were solved.

	Interface function	#tasks	Mem. havoc.	Obj. havoc.	Tool-spec. havoc.
Guest-side TDG	MR.REPORT	10	0	0	5
	SERVTD.WR	10	0	0	7
	SYS.RD	10	0	0	8
	VM.WR	17	0	0	14
	VP.ENTER	18	0	0	12
	VP.VMCALL	10	0	0	8
Host-side TDH	EXPORT.RESTORE	10	3	0	7
	IMPORT.ABORT	9	2	0	7
	MNG.ADDCX	33	5	2	11
	MNG.CREATE	18	3	0	17
	MNG.INIT	33	5	0	11
	MNG.KEY.CONFIG	18	4	0	16
	MNG.KEY.FREEID	17	2	0	16
	MNG.VPFLUSHDONE	21	4	0	19
	MR.FINALIZE	29	3	0	7
	PHYMEM.PAGE.RECLAIM	25	0	0	5
	SYS.CONFIG	29	0	0	8
	SYS.INIT	17	0	0	13
	SYS.KEY.CONFIG	13	10	0	13
	SYS.SHUTDOWN	17	0	0	13
	SYS.UPDATE	25	0	0	19
	VP.ENTER	29	0	0	9
	Overall	418	41	2	245

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Challenges for Evaluated Software Verifiers (1/4)

- Extensive use of nested type punning → frontend failures for several tools

```
union {
    struct {
        uint32_t field_code : 24;
        uint32_t reserved_0 : 8;
    }; // default field code
    struct {
        uint32_t element : 1;     // 0
        uint32_t subleaf : 7;     // 1-7
        uint32_t subleaf_na : 1; // 8
        uint32_t leaf : 7;        // 9-15
        uint32_t leaf_bit31 : 1; // 16
        uint32_t reserved : 15;  // 17-31
    } cpuid_field_code;
};
```

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- Initialization and constraining of complex structures
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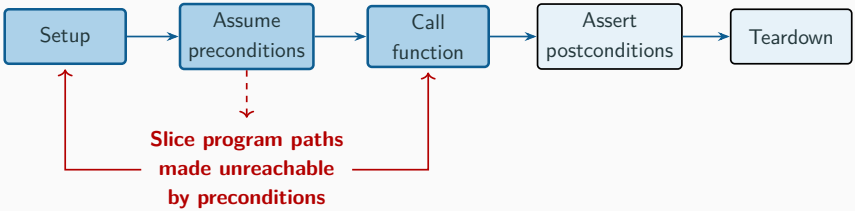
SV-COMP 2026 introduced a new primitive to havoc memory.

Challenges for Evaluated Software Verifiers (3/4)

Limited effectiveness for negative-space safety properties

→ Require "smarter" slicing of unreachable logic and unused variables



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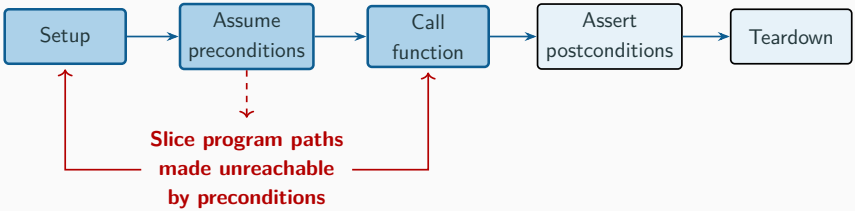

Verification should go hand in hand with harness design!

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- Precise control over memory layout imperative for firmware
  - E.g., ensure sensitive data only written to hardware-protected memory range
  - Compiler attributes `aligned(n)`, `__packed__` common in firmware struct
  - Not widely supported by off-the-shelf verifiers

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- Produced a publicly available benchmark set for firmware verification
  part of SV-Benchmarks and used in SV-COMP 2026
- Motivated the addition of a new primitive for memory havocking in SV-COMP 2026 (`__VERIFIER_nondet_memory`)

Conclusion

A **case study**: six software verifiers applied to **TDX Module**

(22 interface functions, 418 tasks)

- Many verification tasks unsolved
  - Firmware-specific C patterns
  - Symbolic initialization/constraining of complex objects
  - Tools' lack of awareness of harness design
  - Memory layout not well understood by evaluated tools

Future work:

- Property-directed slicing
- Richer properties (e.g., multiple TDs, cross-function)
- LLM-assisted harness generation

Project webpage

INT31 blog post

References i

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Excerpted Specification of TDH.MNG.KEY.CONFIG

Input Operands	
Operand	**Description**
RAX	SEAMCALL instruction leaf number and version
RCX	The physical address of a TDR page (HKID bits must be 0)
Output Operands	
Operand	**Description**
RAX	SEAMCALL instruction return code
Other registers	Unmodified
State-Operand Information	
Operand	**Information**
Trust Domain Root (TDR) page	Explicitly accessed, Read/Write permission, 4KB alignment
Key Encryption Tables (KETs)	Implicitly accessed
Completion-Status Codes (Excerpted)	
Operand	**Description**
TDX_OPERAND_INVALID	An input operand of the interface function is invalid
TDX_LIFECYCLE_STATE_INCORRECT	System in an incorrect lifecycle state
TDX_KEY_GENERATION_FAILED	Failed to generate a random key

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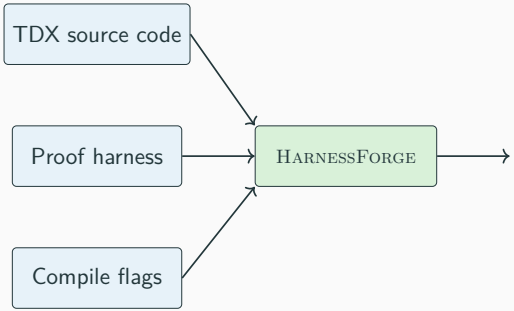
Reachability

Assembling of Verification Tasks




```
[...]

// auto-generated task entry point
void main() {
  hmkc__setup();
  hmkc__invalid_input_rcx__precond();
  hmkc__function_call();
  hmkc__invalid_input_rcx__postcond();
  hmkc__teardown();
}
```

single-file, self-contained

HarnessForge: to appear at FSE 2026