CPV: A Circuit-Based Program Verifier

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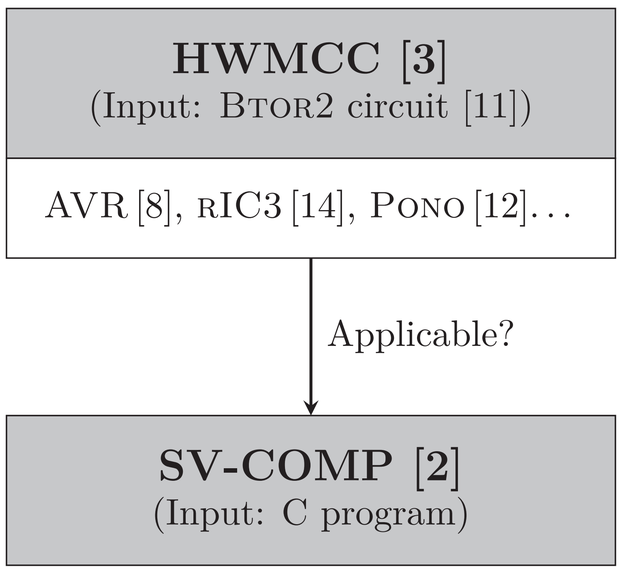
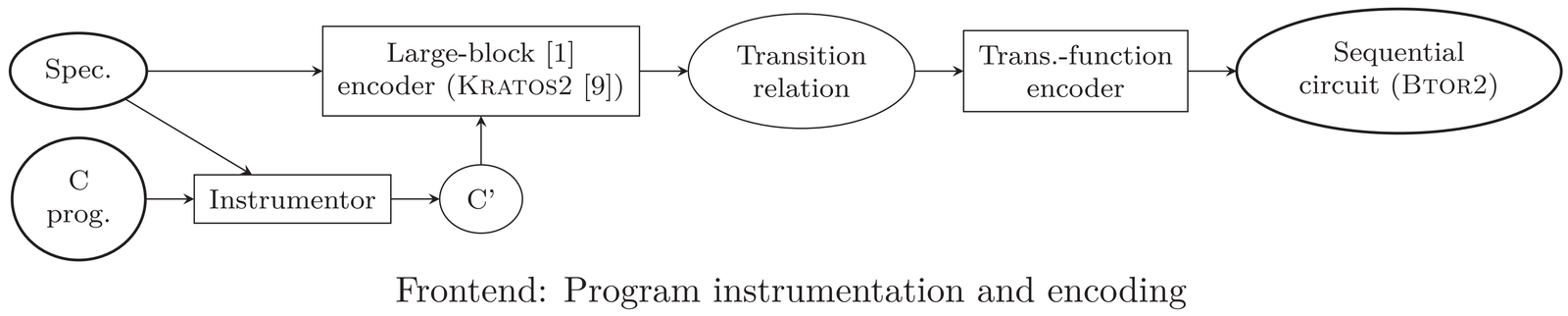
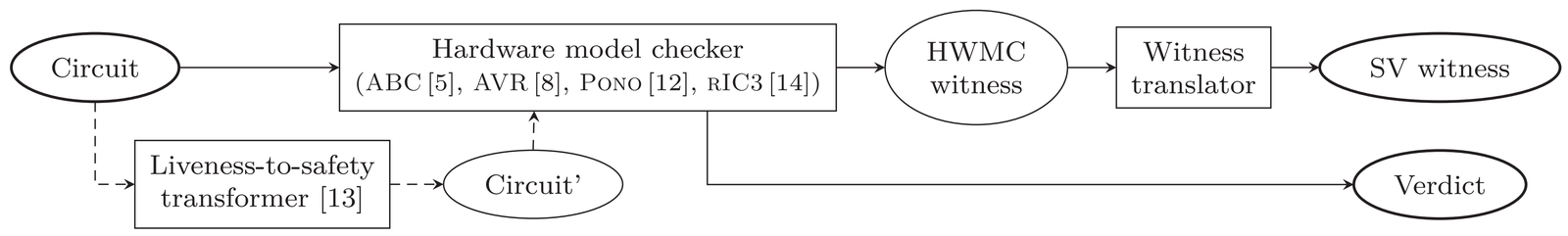
Motivation



CPV's Verification Pipeline



Frontend: Program instrumentation and encoding



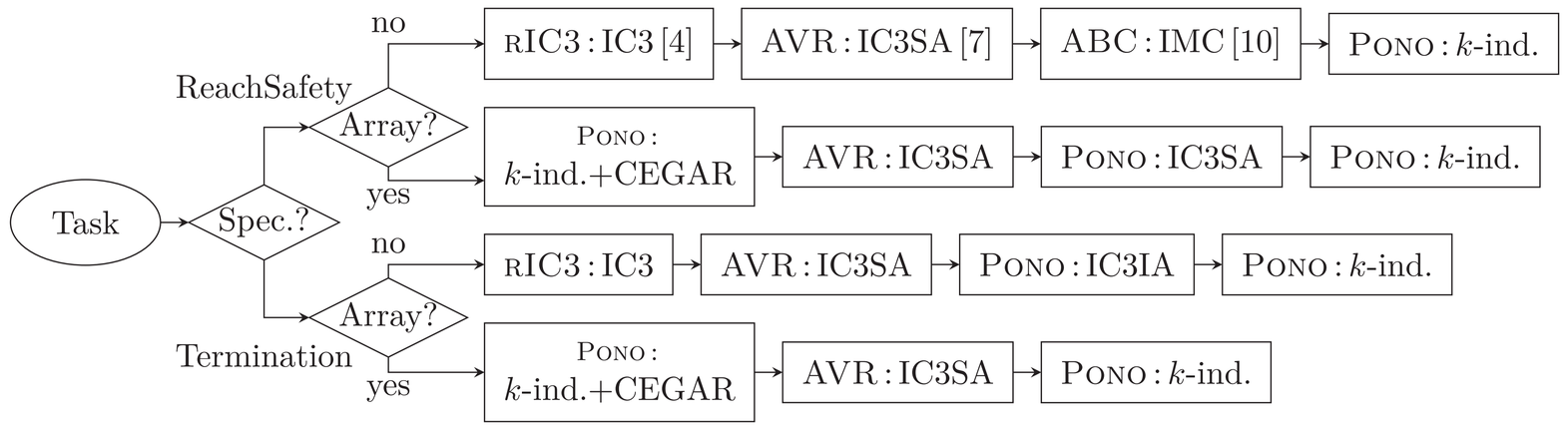
Backend: Model checking and witness translation

Try CPV!

gitlab.com/sosy-lab/software/cpv

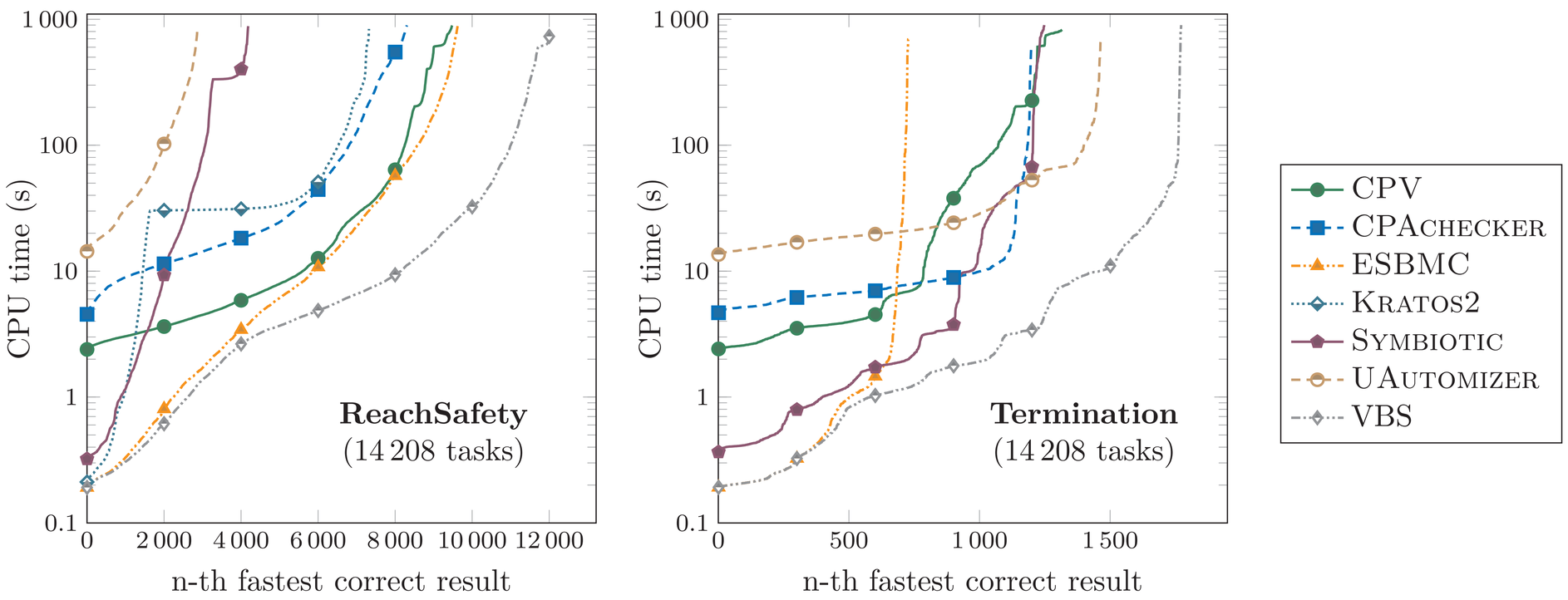
TACAS 2024 [6]

Strategy for SV-COMP 2026



Comparison with State-of-the-Art Software Verifiers

- Benchmark set: SV-COMP 2026 tasks without recursive functions
- Resource limits: 900 s CPU time and 15 GB memory
- Cactus plots show the number of solved tasks, without witness validation or subcategory weighting
- In the comparison, CPV
  - derived the **most proofs** for ReachSafety and
  - found the **most alarms** for Termination



Summary

- Sequential circuits can serve as an intermediate representation for software verification
- Offer various instrumentation, encoding and transformation options
- Leverage powerful word- and bit-level hardware model checkers as backend
- Perform competitively against state-of-the-art verifiers in SV-COMP
- Export violation witnesses in GraphML (v1) and YAML (v2) formats
- Next step: Produce correctness witnesses by translating invariants derived by hardware model checkers

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